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PATENT
Docket No. P1571

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANTS:	JENNIFER WANG MIKE BARSKY	
SERIAL NO.	10/781,353	EXAMINER: ANH D. MAI
FILED:	FEBRUARY 17, 2004	ART UNIT: 2814
CONFIRMATION NO.:	9226	
TITLE:	VIA FORMED IN POLYMER LAYER	

COMMISSIONER FOR PATENTS
P.O. BOX 1450
ALEXANDRIA, VA 22313-1450

AMENDED APPEAL BRIEF

TABLE OF CONTENTS

I. REAL PARTY IN INTEREST

The real party in interest is Northrop Grumman Corporation, the assignee of record.

II. RELATED APPEALS AND INTERFERENCES

None

III. STATUS OF CLAIMS

Claims 1-27 are pending. Non-elected invention, claims 1-20 have been withdrawn. Claims 21-27 are rejected.

IV. STATUS OF AMENDMENTS

After Final Amendment filed April 2, 2007, was acknowledged in the Office communication mailed September 5, 2007. The amendment was acted upon by the examiner and entered.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Reference for support of each element of the claims is in italics and refers to the amended Specification submitted October 26, 2005

Independent Claim 21

A semiconductor structure is etched by releasing a fluoride gas into a chamber, whereby an exposed portion of the hard-mask defining a via hole is etched away. Next, a second etching process is performed that etches the polymer layer by releasing a second fluoride gas into the chamber. This creates the vertical side walls.

21. (Previously Presented) A device including a via produced by the process comprising the steps of:

placing a hard-mask on a polymer layer;
See all of paragraph [0008], all of [0024], Figure 2A

placing a photoresist mask on said hard-mask;
See all of paragraph [0008], all of [0024], Figure 2A

releasing a first fluoride gas into a chamber to etch a hard-mask opening for defining a via hole; and
See all of paragraph [0008], all of [0024], all of [0025], Figure 2B

releasing a second fluoride gas into said chamber to etch an exposed portion of said polymer layer defining said via hole with at least one vertical sidewall,
See all of paragraph [0026], Figure 2C

whereby the via hole comprises an aspect ratio which is greater than 1, and is of substantially the same diameter throughout the depth of the via hole.
See all of paragraph [0027], all of [0030], Figure 2C, Figure 3

Independent Claim 22

A semiconductor structure which has already been etched by releasing a fluoride gas into a chamber, whereby an exposed portion of the hard-mask defining a via is etched away, as well as a second etching process has already been performed that etched the polymer layer by releasing a second fluoride gas into the chamber. This creates the vertical side walls from which a third fluoride gas is released into the chamber whereby the hard-mask is etched away and an exposed portion of the polymer layer at the via-opening is etched away to create the tapered sidewalls.

22. (Previously Presented) A device including a via produced by the process comprising the steps of:

placing in a chamber a semiconductor substrate including a polymer layer defining a sub-micron wide via-opening deposited on said semiconductor substrate,
See all of paragraph [0008], all of [0024], all of [0029], all of [0031], Figure 2A

and a hard-mask defining said sub-micron wide via-opening deposited on said polymer layer;
See all of paragraph [0008], all of [0024], all of [0029], all of [0031], Figure 2A

whereby the via comprises an aspect ratio which is greater than 1, and is of substantially the same diameter throughout at least one-half the depth of the via;
See all of paragraph [0027], all of [0030], all of [0034], Figure 2C, Figure 3, Figure 4A

releasing a third fluoride gas into said chamber to etch said hard-mask
See all of paragraph [0031], all of [0032], all of [0033], all of [0035]

and an exposed portion of said polymer layer proximal to said sub-micron wide via-opening thereby creating at least one tapered sidewall within a via.
See all of paragraph [0032], all of [0033], Figure 4B, Figure 5

Claim 23 depending from Claim 22
A semiconductor structure which has already been etched by releasing a fluoride gas into a chamber, whereby an exposed portion of the hard-mask defining a via is etched away, as well as a second etching process has already been performed that etched the polymer layer by releasing a second fluoride gas into the chamber. This creates the vertical side walls from which a third fluoride gas is then released into the chamber whereby the hard-mask is etched away and an exposed portion of the polymer layer at the via-opening is etched away to create the tapered sidewalls that are at least one-third the depth of the via.

23. (Previously Presented) A device as recited in Claim 22 wherein the via includes a tapered sidewall extending at least one-third of the depth thereof.
See all of paragraph [0036]

Claim 24 depending from Claim 22
A semiconductor structure which has already been etched by releasing a fluoride gas into a chamber, whereby an exposed portion of the hard-mask defining a via is etched away, as well as a second etching process has already been performed that etched the polymer layer by releasing a second fluoride gas into the chamber. This creates the vertical side walls from which a third fluoride gas is then released into the chamber whereby the hard-mask is etched away and an exposed portion of the polymer layer at the via-opening is etched away to create the tapered sidewalls that are up to one half the depth of the via.

24. (Previously Presented) A device as recited in Claim 22 wherein the via includes a tapered sidewall extending up to one-half of the depth thereof.
See all of paragraph [0036]

Independent Claim 25
A semiconductor structure is etched by releasing a fluoride gas into a chamber, whereby an exposed portion of the hard-mask defining a via hole is etched away. Next, a second etching process is performed that etches the polymer layer by releasing a second fluoride gas into the chamber. This creates the vertical side walls. A third fluoride gas is then released into the chamber whereby the hard-mask is etched away and an exposed portion of the polymer layer at the via-opening is etched away to create the tapered sidewalls.

25. (Previously Presented) A device including a via produced by the process comprising the steps of:

placing a hard-mask on a polymer layer;
See all of paragraph [0008], all of [0024], Figure 2A

placing a photoresist mask on said hard-mask;
See all of paragraph [0008], all of [0024], Figure 2A

releasing a first fluoride gas into a chamber to etch a hard-mask opening for defining a via hole;
See all of paragraph [0008], all of [0024], all of [0025], Figure 2B

releasing a second fluoride gas into said chamber to etch an exposed portion of said polymer layer defining said via hole with at least one vertical sidewall and a sub-micron wide via-opening;
See all of paragraph [0026], Figure 2C

whereby the via hole comprises an aspect ratio which is greater than 1, and is of substantially the same diameter throughout at least one-half the depth of the via hole;
See all of paragraph [0027], all of [0030], all of [0034], Figure 2C, Figure 3, Figure 4A

releasing a third fluoride gas into said chamber to etch said hard-mask and an exposed portion of said polymer layer proximal to said sub-micron wide via-opening
See all of paragraph [0031], all of [0032], all of [0033], all of [0035]

thereby creating at least one tapered sidewall within a via hole.
See all of paragraph [0032], all of [0033], Figure 4B, Figure 5

Claim 26 depending from Claim 25

A semiconductor structure is etched by releasing a fluoride gas into a chamber, whereby an exposed portion of the hard-mask defining a via hole is etched away. Next, a second etching process is performed that etches the polymer layer by releasing a second fluoride gas into the chamber. This creates the vertical side walls. A third fluoride gas is then released into the chamber whereby the hard-mask is etched away and an exposed portion of the polymer layer at the via-opening is etched away to create the tapered sidewalls that are at least one-third the depth of the via.

26. (Previously Presented) A device as recited in Claim 25 wherein the via includes a tapered sidewall extending at least one-third of the depth thereof.
See all of paragraph [0036]

Claim 27 depending from Claim 25

A semiconductor structure is etched by releasing a fluoride gas into a chamber, whereby an exposed portion of the hard-mask defining a via hole is etched away. Next, a second etching process is performed that etches the polymer layer by releasing a second fluoride gas into the chamber. This creates the vertical side walls. A third fluoride gas is then released into the chamber whereby the hard-mask is etched away and an exposed portion of the polymer layer at the via-opening is etched away to create the tapered sidewalls that are up to one half the depth of the via.

27. (Previously Presented) A device as recited in Claim 25 wherein the via includes a tapered sidewall extending up to one-half of the depth thereof.
See all of paragraph [0036]

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

(1) Whether claim 22 is unpatentable for being informal.

(2) Whether claims 21, 22, and 25 are unpatentable under 35 U.S.C. 102(b) as being anticipated by Lin (U.S. Patent No. 6,515,369) of record.

(3) Whether claim 21 is unpatentable under 35 U.S.C. 103(a) over Yu *et al.* (U.S. Patent No. 6,004,883) in view of Lin (U.S. Pub. No. 2002/0068441) all of record.

(4) Whether claim 21 is unpatentable under 35 U.S.C. 103(a) over Yu *et al.* (U.S. Patent No. 6,004,883) in view of the feature not taught by Yu, as an obvious matter of design choice.

(5) Whether claim 21 is unpatentable under 35 U.S.C. 103(a) over Yu *et al.* (U.S. Patent No. 6,004,883) in view of the feature not taught by Yu, not being disclosed in the specification as either *critical in nature* or unexpected results arising therefrom.

(6) Whether claim 21 is unpatentable under 35 U.S.C. 103(a) over Yu *et al.* (U.S. Patent No. 6,004,883) in view of the feature not taught by Yu, as within the purview of one having ordinary skill in the art.

(7) Whether claims 23, 24, 26, and 27 are unpatentable under 35 U.S.C. 103(a) over Lin (U.S. Patent No. 6,515,369) in view of the feature not taught by Lin, not being disclosed in the specification as either *critical in nature* or unexpected results arising therefrom.

(8) Whether claims 23, 24, 26, and 27 are unpatentable under 35 U.S.C. 103(a) over Lin (U.S. Patent No. 6,515,369) in view of the feature not taught by Lin, as within the purview of one having ordinary skill in the art.

VII. ARGUMENTS

(1) Objection of claim 22 for being informal

Claim 22 was objected to because of the following informalities: line 4 recites: "via-opening" and line 8 recites: "via hole". Appellants assert that "via hole" is not recited in claim 22, therefore, this objection is unworkable.

(2) Rejection under 35 U.S.C. 102(b) over Lin (U.S. Patent No. 6,515,369)

(a) Claim 21

Claim 21 has been rejected under 35 U.S.C. 102(b) as being anticipated by Lin '369. Appellants respectfully traversed this rejection. The Examiner has idealized the drawings in Lin to conform to what he believes the invention to be in Lin. Nowhere within Lin does it teach the elements of Claim 21. The Examiner cites Figure 5a, however Lin is silent on teaching how to achieve this complicated process. Appellants novel process results in a device that has never before been accomplished on a sub-micron or micron level. The idealized drawing does not meet the requirements of 35 U.S.C. 102(b) because the Appellants invention was not patented or described in Lin. A crude drawing in Lin that represents an entirely different concept and invention is being used by the Examiner to erroneously reject Appellants invention.

(b) Claim 22

Claim 22 has been rejected under 35 U.S.C. 102(b) as being unpatentable in view of Lin '369. The Appellants respectfully traversed this rejection. Lin Figure 10 which is cited by the Examiner has been idealized by the Examiner into something that it is not. It does not even show the elements as claimed in the present invention.

The apertures formed by Lin, as idealized by the Examiner, are structurally different than the vias of Claim 22. The vias of Claim 22 are dimensionally accurate to micron and sub-micron levels, having substantially the same diameter throughout the depth of the via other than at the tapering at the via-opening. These tapered sidewalls are only etched at the via-opening and are not throughout the depth of the via. The rest of the via hole has vertical sidewalls. Lin is silent as to the tapering and verticality of the sidewalls of such vias. The Examiner has cited Figure 10, however there is no disclosure that there is tapering of the sidewall, much less how to achieve it. Appellants invention is unobvious because it presents a novel way to etch vertical sidewalls in a via along with a tapered opening, such that via openings are not overlapping and damaging adjacent features. This novel process results in a device that has never before been accomplished on a sub-micron or micron level. Nowhere within Lin '369 does it teach the elements of Claim 22.

(c) Claim 25

Claim 25 has been rejected under 35 U.S.C. 102(b) as being anticipated by Lin '369. Appellants respectfully traverse this rejection. The Examiner has idealized the drawings in Lin to conform to what he believes the invention to be in Lin. Nowhere within Lin '369 does it teach the elements of Claim 25. Lin Figure 10 which is cited by the Examiner does not even show the elements as claimed in the present invention. The Examiner has failed to establish a prima facie case for a 35 USC 102(b) rejection, since Lin '369 fails to patent or describe the Appellants invention.

Appellants believe that they have successfully overcome the rejection based on 35 U.S.C. 102(b) by persuasively arguing that the claims are patentably distinguishable from the prior art.

(3) Rejection of claim 21 under 35 U.S.C. 103(a) over Yu *et al.* (U.S. Patent No. 6,004,883) in view of Lin (U.S. Pub. No. 2002/0068441)

Claim 21 has been rejected, under 35 U.S.C. §103(a) as being unpatentable over Yu et al (U.S. Patent No. 6,004,883) in view of Lin (U.S. Pub. No. 2002/0068441). The Appellants respectfully traverse this rejection.

Addressing the cited art, Yu merely teaches a method for forming a via whereby the resulting aperture comprises a second trench corresponding with a first trench and at least a portion of a first via. The method taught by Yu is unable to etch a deep via hole having substantially the same diameter throughout the depth of the via. As stated in Yu at col 4 lines 48-50, "The aperture comprises:(1) a second trench corresponding with the first trench; and (2) at least a portion of the first via." The aperture that results is staggered and does not have smooth vertical sidewalls. There is absolutely no consistent verticality of the walls of the via hole, as can be seen in the figures. This results in an entirely different device than that claimed in the present invention. The vias of Claim 21 are dimensionally accurate micron and sub-micron via holes of substantially the same diameter throughout the depth of the via hole due to the prescribed method of the present invention. The via hole that is produced has vertical side walls, see paragraph [0027] of the amended Specification submitted October 26, 2005 for support. There is no teaching, showing or suggestion of verticality of the sidewalls of the via hole in Yu which would result in the present invention's via hole having substantially the same diameter throughout the depth of the via hole. The present invention is unobvious in view of Yu.

Lin may disclose a via with an aspect ratio greater than one, however there is no teaching, showing or suggestion of vertical sidewalls of the via hole which would result in a via hole having substantially the same diameter throughout it's depth. Since Yu does not make the present invention obvious for the reasons stated above, adding Lin merely for the aspect ratio would still not accomplish the structure of the claimed device.

There is no suggestion, teaching or motivation found in the references to practice Appellants claimed invention. See *Ex parte Clapp*, 227 USPQ 972, 973 (Bd. Pat. App. & Inter. 1985) ("To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or impliedly suggest the claimed invention or the Examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references."). Even if the Examiner's position regarding the art were taken as correct, he has failed to point out where there is a suggestion or motivation to combine these references. Since there was no suggestion or motivation in the references, success cannot be expected to achieve what the Examiner believes is disclosed in these references. Additionally, the level of skill in the art cannot be relied upon to provide the suggestion to combine references. *Al-Site Corp. v. VSI Int'l Inc.*, 174 F.3d 1308, 50 USPQ2d 1161 (Fed. Cir. 1999). Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. There is no teaching or suggestion in the cited art of each of Appellants process and device elements, which the Examiner points to. Therefore, a prima facie case of obviousness has not been proven. Appellants respectfully request that this ground for rejection on this basis be withdrawn and that Claim 21 be passed to allowance.

(4) Rejection of claim 21 under 35 U.S.C. 103(a) over Yu *et al.* (U.S. Patent No. 6,004,883) in view of the feature not taught by Yu, as an obvious matter of design choice

Appellants have traversed the Examiner's rejection as an obvious matter of design choice to define a via having an aspect ratio greater than 1. The size modifications within this technology field are cutting edge and continually evolving, that is the field of art, to create more precise semiconductor devices. The Examiner has failed to cite any art which can support his argument. Under 37 CFR 1.113, official notice without documentary evidence to support an Examiner's conclusion should be rare, especially when an application is under final rejection. Official notice unsupported by documentary evidence should only be taken by the Examiners where the facts asserted to be well-known, or to be common knowledge in the art, are capable of instant and unquestionable demonstration as being well-known. Appellants assert that instant and unquestionable demonstration of this knowledge is not present here. Therefore, the Examiner has not made a prima facie case of obviousness.

(5) Rejection of claim 21 under 35 U.S.C. 103(a) over Yu *et al.* (U.S. Patent No. 6,004,883) in view of the feature not taught by Yu, not being disclosed in the specification as either *critical in nature* or unexpected results arising therefrom

In response to the Examiner stating that there is no disclosure of either the *critical nature of the claimed aspect ratio of greater than 1* or any unexpected results arising therefrom, the Appellants respectfully traversed this argument presented by the Examiner. Disclosure can be found at paragraph [0027] of the amended Specification submitted October 26, 2005.

(6) Rejection of claim 21 under 35 U.S.C. 103(a) over Yu *et al.* (U.S. Patent No. 6,004,883) in view of the feature not taught by Yu, as within the purview of one having ordinary skill in the art

Appellants traversed the rejection that the novel process that results in the claimed structure would involve a mere change in the size of a component, and that such change is generally recognized as being within the level of ordinary skill in the art.

The Examiner is held to the same standards as the Board of Patent Appeals. Precedent case law dictates that "the Board cannot simply reach conclusions based on its own understanding or experience - or on its assessment of what would be basic knowledge or common sense. Rather, the Board must point to some concrete evidence in the record in support of these findings." *Zurko*, 258 F.3d at 1385, 59 USPQ2d at 1697. The Examiner has failed to cite any art which can support this argument of being generally recognized within the level of ordinary skill in the art at the time the invention was filed.

(7) Rejection under 35 U.S.C. 103(a) over Lin (U.S. Patent No. 6,515,369) in view of the feature not taught by Lin, not being disclosed in the specification as either *critical in nature* or unexpected results arising therefrom

(a) Claims 23 and 24

In response to the Examiner stating that there is no disclosure of either the *critical nature of the claimed extending of the tapered sidewall in the range from one-third to one half* or any unexpected results arising therefrom, the Appellants have respectfully traversed this argument presented by the Examiner. On the contrary, notwithstanding *In re Saunders,* 444 F.2d 599, 607, 170 USPQ 213, 220 (CCPA 1971), from the beginning the Appellants have supported this claim in the specification at paragraphs [0027], [0033], and [0036] in the amended Specification submitted October 26, 2005. The Examiner is failing to understand the technology and where in the specification disclosure can be found.

(b) Claims 26 and 27

Similarly in response to the Examiner stating that there is no disclosure of either the *critical nature of the claimed extending of the tapered sidewall in the range from one-third to one half* or any unexpected results arising therefrom, the Appellants have respectfully traversed this argument presented by the Examiner. Disclosure can be found at paragraphs [0027], [0033], and [0036] in the amended Specification submitted October 26, 2005.

(8) Rejection under 35 U.S.C. 103(a) over Lin (U.S. Patent No. 6,515,369) in view of the feature not taught by Lin, as within the purview of one having ordinary skill in the art

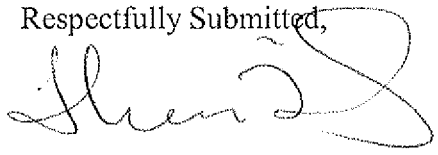
(a) Claims 23 and 24

Appellants have traversed that the novel process that results in the claimed structure would involve a mere change in the size of a component, and that such change is generally recognized as being within the level of ordinary skill in the art. The Examiner has failed to cite any art which can support this argument of being generally recognized within the level of ordinary skill in the art at the time the invention was filed. Appellants refer to the above arguments in paragraph (6).

(b) Claims 26 and 27

Appellants have traversed that the novel process that results in the claimed structure would involve a mere change in the size of a component, and that such change is generally recognized as being within the level of ordinary skill in the art. The Examiner has failed to cite any art which can support this argument of being generally recognized within the level of ordinary skill in the art at the time the invention was filed. Appellants refer to the above arguments in paragraph (6).

Respectfully Submitted,



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CLAIMS APPENDIX

1. (Withdrawn) A via etching process for a polymer layer deposited on a semiconductor substrate comprising said steps of:
placing a hard-mask on said polymer layer;
placing a photoresist mask on said hard-mask;
releasing a first fluoride gas into a chamber to etch a hard-mask opening for defining said via hole; and
releasing a second fluoride gas into said chamber to etch an exposed portion of said polymer layer defining said via hole with vertical sidewalls.

2. (Withdrawn) A via etching process as recited in Claim 1, wherein said first fluoride gas comprises trifluoromethane and argon.

3. (Withdrawn) A via etching process as recited in Claim 1, wherein said first fluoride gas comprises a volume ratio of one part trifluoromethane to one part argon.

4. (Withdrawn) A via etching process as recited in Claim 1, wherein said step of releasing first fluoride gas further includes applying bias power within the range of approximately 25 Watts to approximately 32 Watts.

5. (Withdrawn) A via etching process as recited in Claim 1, wherein said step of releasing first fluoride gas further includes applying pulse-modulated power comprising inductively coupled plasma power within the range of approximately 725 Watts to approximately 755 Watts.

6. (Withdrawn) A via etching process as recited in Claim 1, wherein said said step of releasing first fluoride gas further includes for approximately three to seven minutes doing all the following: applying a first fluoride gas comprising an equal ratio of trifluoromethane and argon, applying a pressure of approximately 10 milli-Torr, applying a temperature of approximately 20 degrees C, applying pulse-modulated power comprising inductively coupled plasma power within the range of approximately 725 Watts to approximately 755 Watts, and applying bias power within the range of approximately 25 Watts to approximately 32 Watts.

7. (Withdrawn) A via etching process as recited in Claim 1, wherein said second fluoride gas comprises Sulfur Hexafluoride and Oxygen.

8. (Withdrawn) A via etching process as recited in Claim 1, wherein said second fluoride gas comprises Sulfur Hexafluoride and Oxygen, wherein said volume ratio of gases is 1 part Sulfur Hexafluoride to 3 parts Oxygen.

9. (Withdrawn) A via etching process as recited in Claim 1, wherein said polymer layer etching step further comprises applying bias power within the range of approximately 57 Watts to approximately 62 Watts.

10. (Withdrawn) A via etching process as recited in Claim 1, wherein step of releasing a second fluoride gas further includes applying pulse-modulated power comprising inductively coupled plasma power within the range of approximately 475 Watts to approximately 505 Watts.

11. (Withdrawn) A via etching process as recited in Claim 1, wherein step of releasing a second fluoride gas further includes for approximately one and half minutes to six minutes doing all the following: applying a second fluoride gas comprising Sulfur Hexafluoride and Oxygen, wherein said ratio of gases is 1 part Sulfur Hexafluoride to 3 parts Oxygen with an associated pressure of approximately 5 milli-Torr, applying temperature of approximately 20 degrees C, applying pulse-modulated power comprising inductively coupled plasma power with the range of approximately 475 Watts to approximately 505 Watts, and applying bias power comprising a bias power with the range of approximately 25 Watts to approximately 32 Watts.

12. (Withdrawn) A via etching process as recited in Claim 1, wherein said polymer layer is benzocyclobutene polymer.

13. (Withdrawn) A via etching process as recited in Claim 1, wherein said polymer layer is a material with a dielectric constant less than 3.

14. (Withdrawn) An etch process as recited in Claim1, wherein said semiconductor substrate is chosen from the group consisting of Indium Phosphide and Gallium Arsenide.

15. (Withdrawn) A via etching process for a polymer layer on a semiconductor substrate comprising the steps of:

placing in a chamber said semiconductor substrate including a polymer layer defining a sub-micron wide via-opening deposited on said semiconductor substrate, and a hard-mask defining said sub-micron wide via-opening deposited on said polymer layer;

releasing a third fluoride gas into said chamber;

applying bias power within the range of approximately 105 Watts to approximately 120 Watts;

applying pulse-modulated power within the range of approximately 725 Watts to approximately 755 Watts;

pressurizing said third fluoride gas within a range of approximately 5 milli-Torr to approximately 20 milli-Torr; and

continuing the above steps until etching said hard-mark and an exposed portion of said polymer layer proximal to said sub-micron wide via-opening creating tapered sidewalls.

16. (Withdrawn) A via etching process as recited in Claim 15, wherein said third fluoride gas comprises trifluoromethane and argon.

17. (Withdrawn) A via etching process as recited in Claim 15, wherein said third fluoride gas comprises a volume ratio of one part trifluoromethane to one part argon.

18. (Withdrawn) A via etching process as recited in Claim 15, wherein said continuing the above steps within the range of approximately three minutes to approximately seven minutes.

19. (Withdrawn) A via etching process as recited in Claim 15, wherein said polymer layer is benzocyclobutene polymer.

20. (Withdrawn) A via etching process as recited in Claim 15, wherein said polymer layer is a material with a dielectric constant less than 3 and has an etch rate 10 times slower than that of said hard-mask layer.

21. (Previously Presented) A device including a via produced by the process comprising the steps of:
placing a hard-mask on a polymer layer;
placing a photoresist mask on said hard-mask;
releasing a first fluoride gas into a chamber to etch a hard-mask opening for defining a via hole; and
releasing a second fluoride gas into said chamber to etch an exposed portion of said polymer layer defining said via hole with at least one vertical sidewall,
whereby the via hole comprises an aspect ratio which is greater than 1, and is of substantially the same diameter throughout the depth of the via hole.

22. (Previously Presented) A device including a via produced by the process comprising the steps of:
placing in a chamber a semiconductor substrate including a polymer layer defining a sub-micron wide via-opening deposited on said semiconductor substrate, and a hard-mask defining said sub-micron wide via-opening deposited on said polymer layer;
whereby the via comprises an aspect ratio which is greater than 1, and is of substantially the same diameter throughout at least one-half the depth of the via;
releasing a third fluoride gas into said chamber to etch said hard-mask and an

exposed portion of said polymer layer proximal to said sub-micron wide via-opening thereby creating at least one tapered sidewall within a via.

23. (Previously Presented) A device as recited in Claim 22 wherein the via includes a tapered sidewall extending at least one-third of the depth thereof.

24. (Previously Presented) A device as recited in Claim 22 wherein the via includes a tapered sidewall extending up to one-half of the depth thereof.

25. (Previously Presented) A device including a via produced by the process comprising the steps of:

placing a hard-mask on a polymer layer;

placing a photoresist mask on said hard-mask;

releasing a first fluoride gas into a chamber to etch a hard-mask opening for defining a via hole;

releasing a second fluoride gas into said chamber to etch an exposed portion of said polymer layer defining said via hole with at least one vertical sidewall and a sub-micron wide via-opening;

whereby the via hole comprises an aspect ratio which is greater than 1, and is of substantially the same diameter throughout at least one-half the depth of the via hole;

releasing a third fluoride gas into said chamber to etch said hard-mask and an exposed portion of said polymer layer proximal to said sub-micron wide via-opening thereby creating at least one tapered sidewall within a via hole.

26. (Previously Presented) A device as recited in Claim 25 wherein the via includes a tapered sidewall extending at least one-third of the depth thereof.

27. (Previously Presented) A device as recited in Claim 25 wherein the via includes a tapered sidewall extending up to one-half of the depth thereof.

EVIDENCE APPENDIX

Lin (U.S. Patent No. 6,515,369)

Yu et al. (U.S. Patent No. 6,004,883)

Lin (U.S. Pub. No. 2002/0068441)

US006515369B1

(12) **United States Patent**
Lin

(10) **Patent No.: US 6,515,369 B1**
(45) **Date of Patent: Feb. 4, 2003**

(54) **HIGH PERFORMANCE SYSTEM-ON-CHIP USING POST PASSIVATION PROCESS**

(75) Inventor: **Mou-Shiung Lin**, Hsinchu (TW)

(73) Assignee: **Megic Corporation**, Hsin-chu (TW)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/156,412**

(22) Filed: **May 28, 2002**

Related U.S. Application Data

(62) Division of application No. 09/970,005, filed on Oct. 3, 2001.

(51) **Int. Cl.**[7] **H01L 23/12**
(52) **U.S. Cl.** **257/773**; 257/774; 257/724
(58) **Field of Search** 257/773, 774, 257/724, 700, 300; 438/616, 617, 614

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5,884,990	A *	3/1999	Burghartz et al.	336/200
6,008,102	A *	12/1999	Alford et al.	438/381

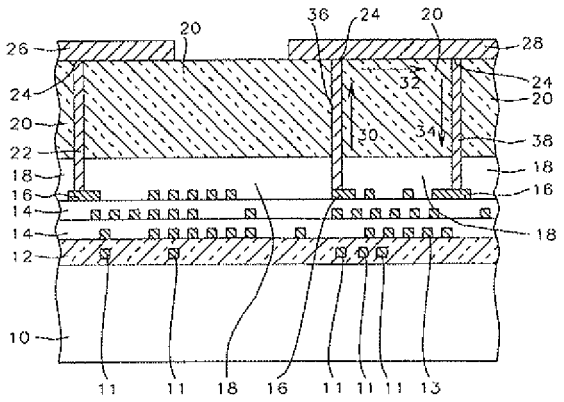
* cited by examiner

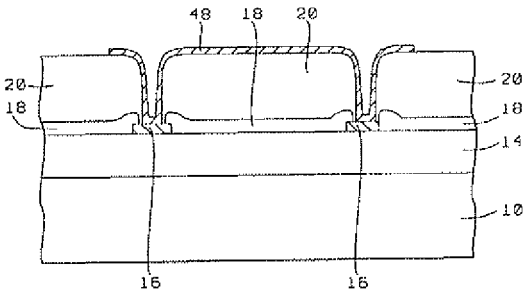
Primary Examiner—Chandra Chaudhari
Assistant Examiner—Yennhu B. Huynh
(74) *Attorney, Agent, or Firm*—George O. Saile; Stephen B. Ackerman

(57) **ABSTRACT**

The present invention extends the above referenced continuation-in-part application by in addition creating high quality electrical components, such as inductors, capacitors or resistors, on a layer of passivation or on the surface of a thick layer of polymer. In addition, the process of the invention provides a method for mounting discrete electrical components at a significant distance removed from the underlying silicon surface.

10 Claims, 11 Drawing Sheets





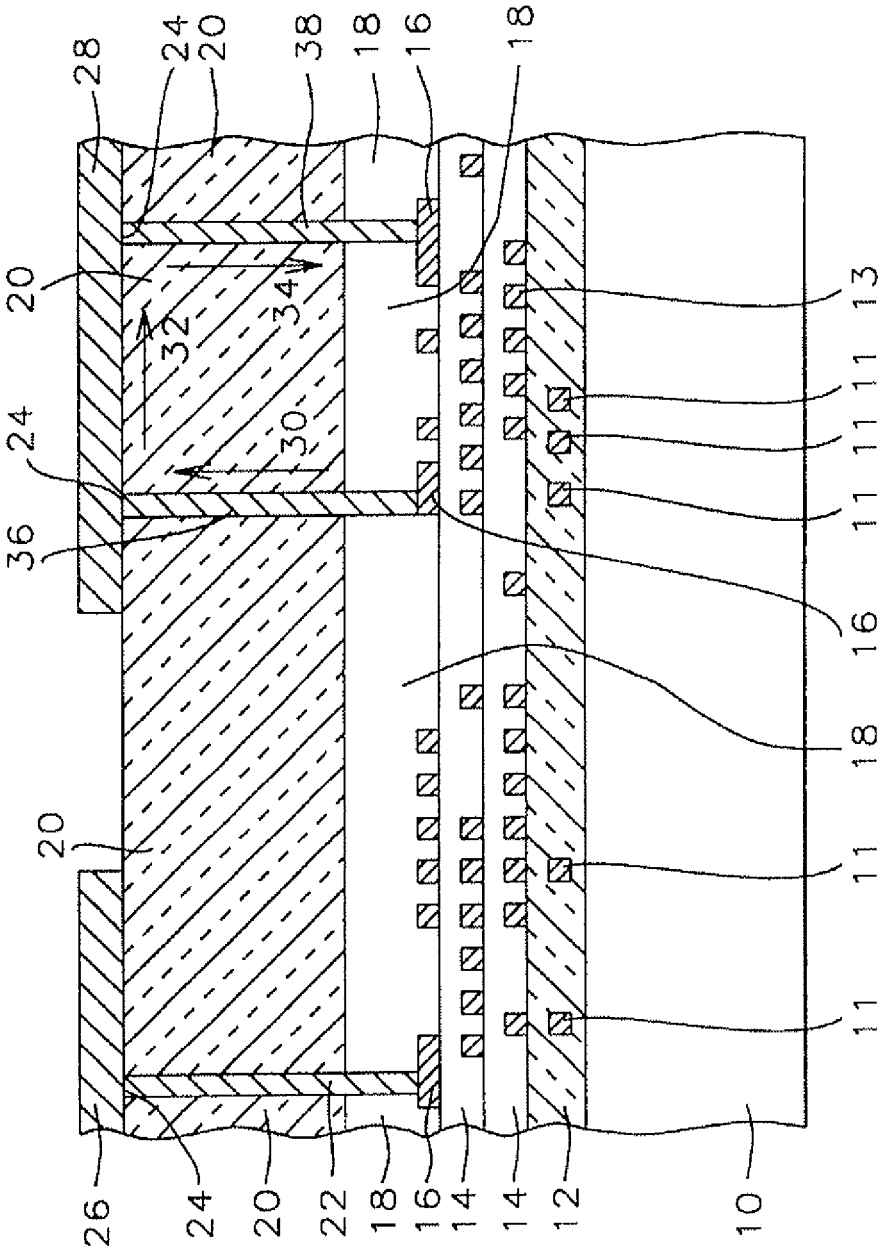

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FIG. 1

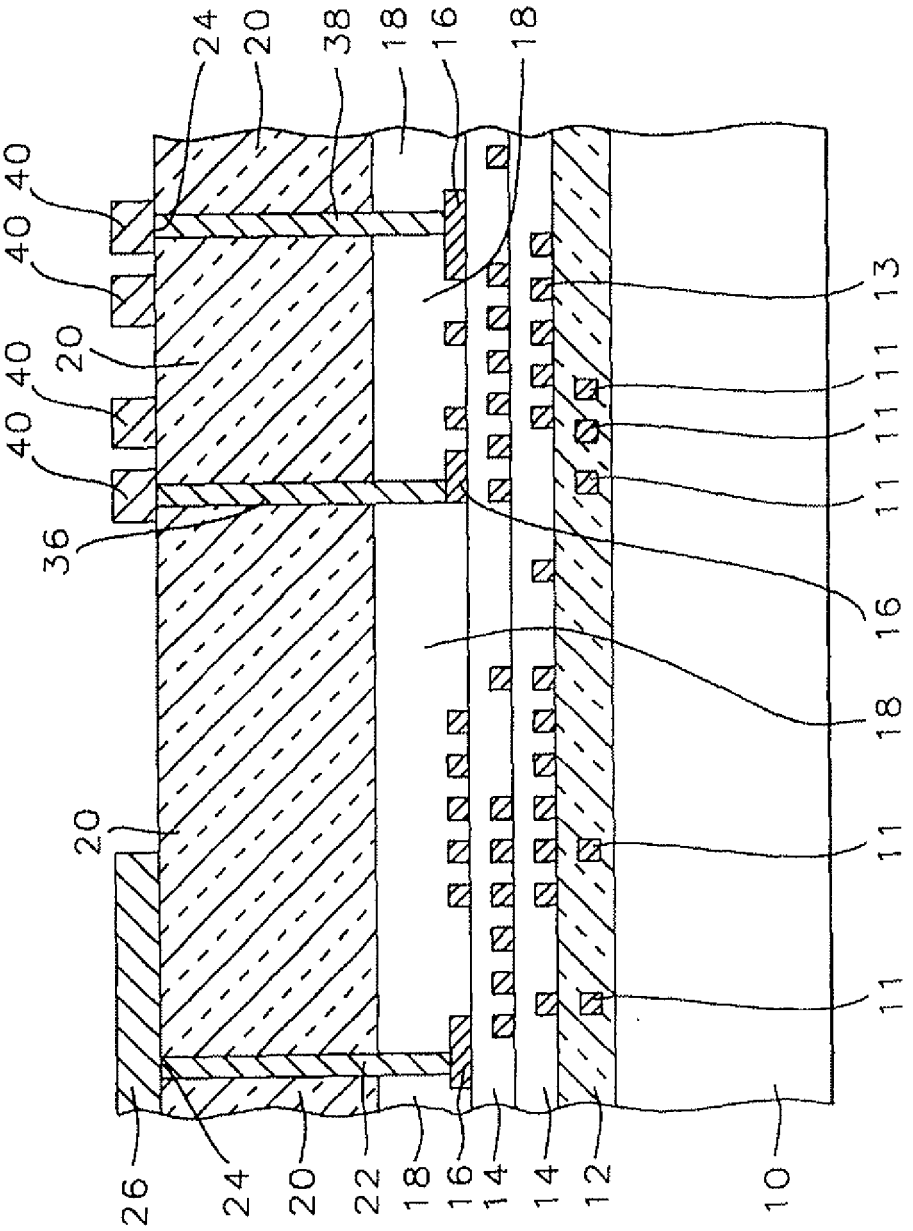
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FIG. 2

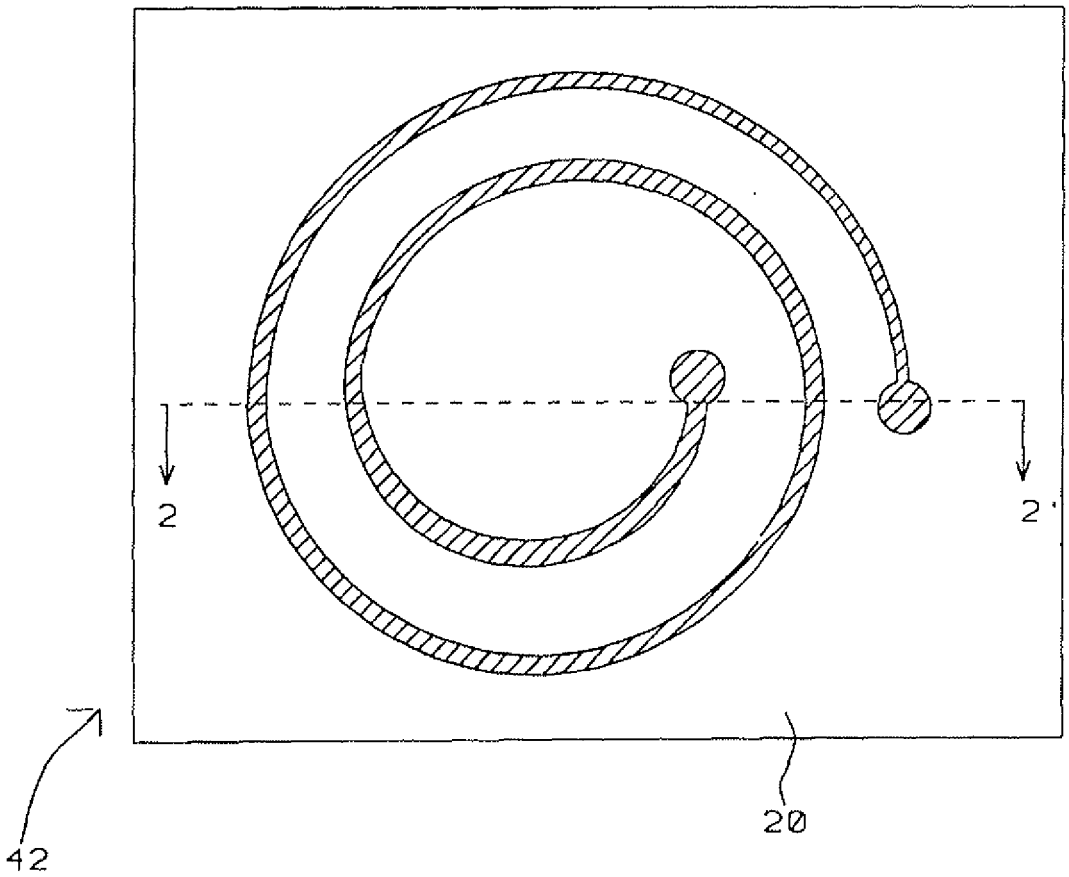

FIG. 3

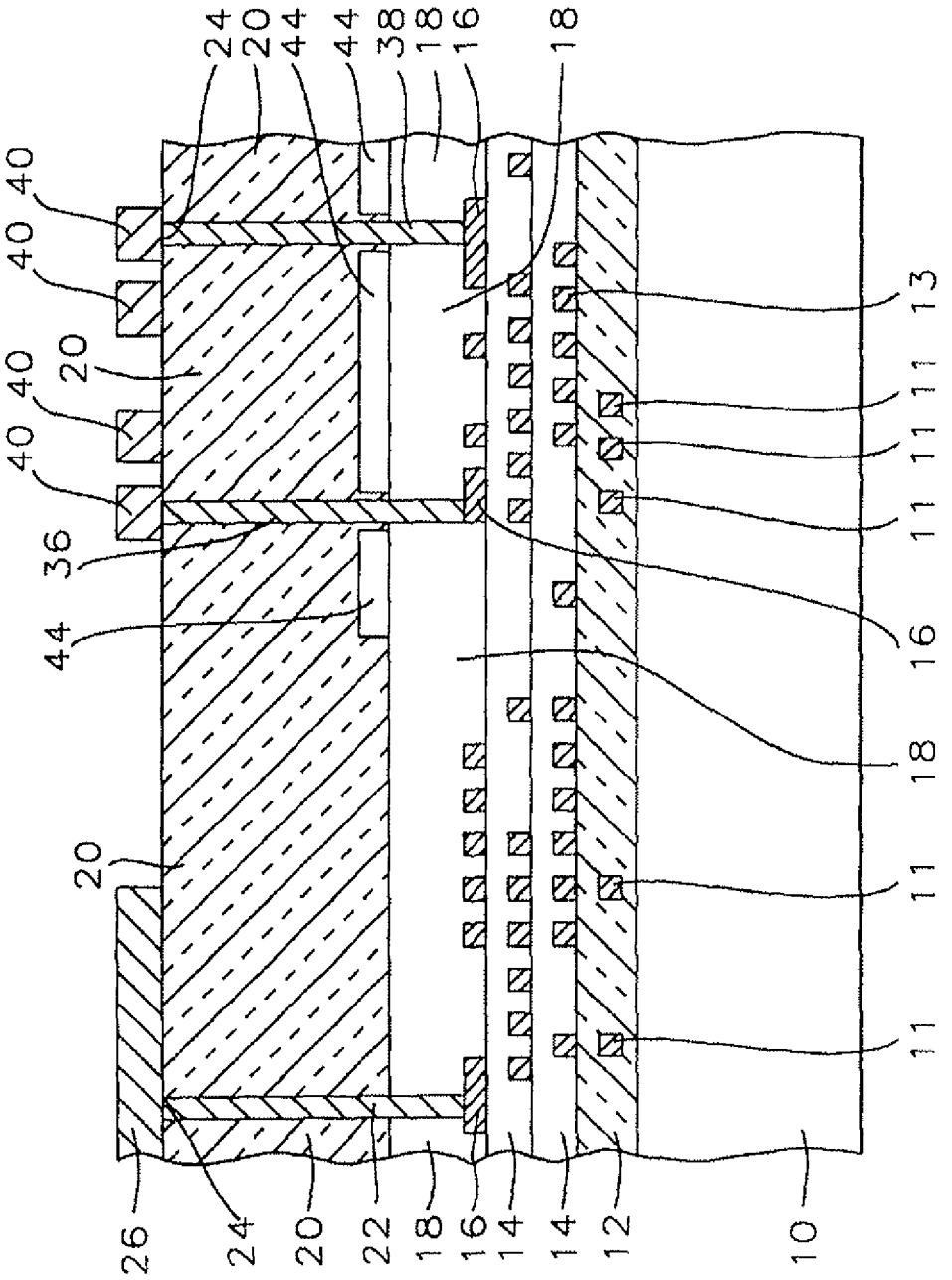
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FIG. 4

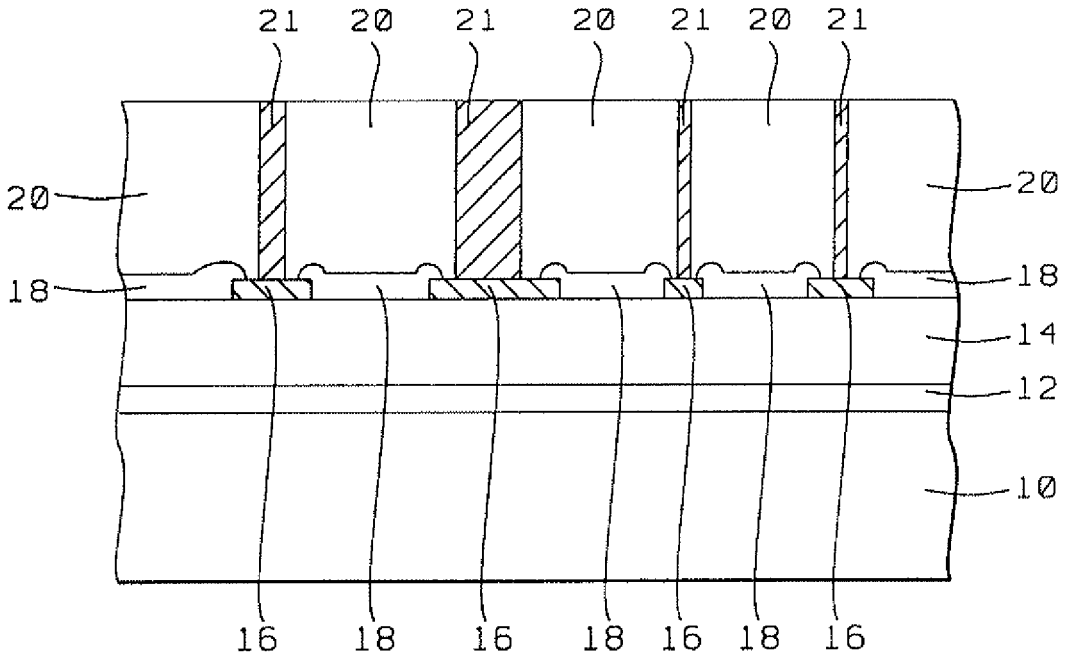
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FIG. 5a

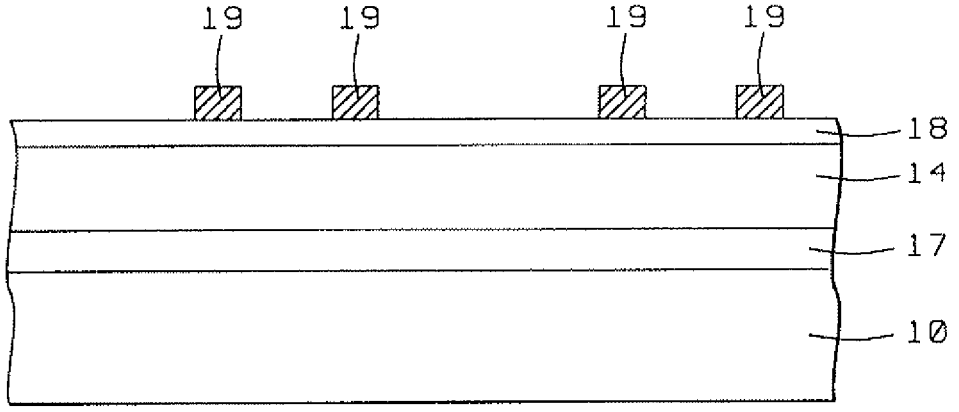
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FIG. 5b

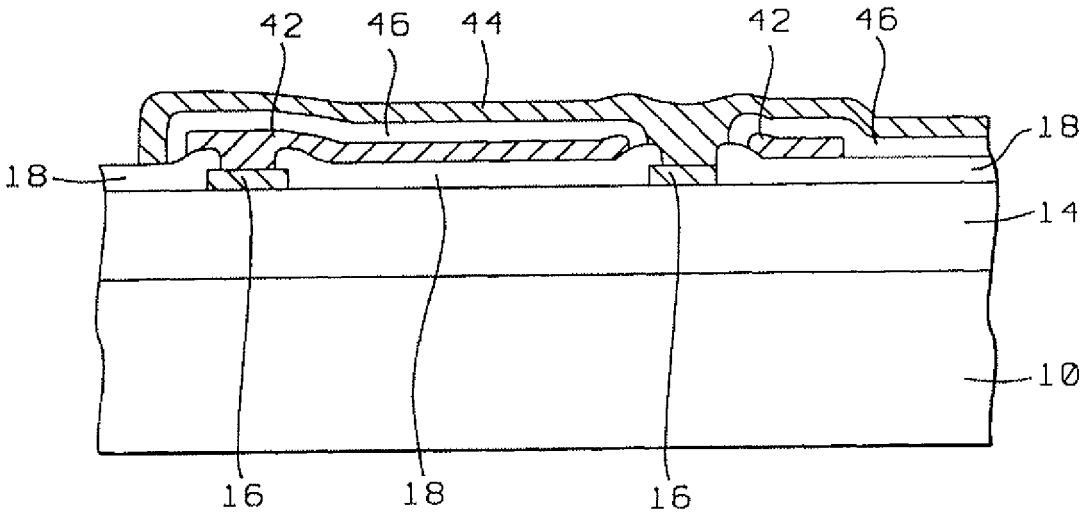

FIG. 6a

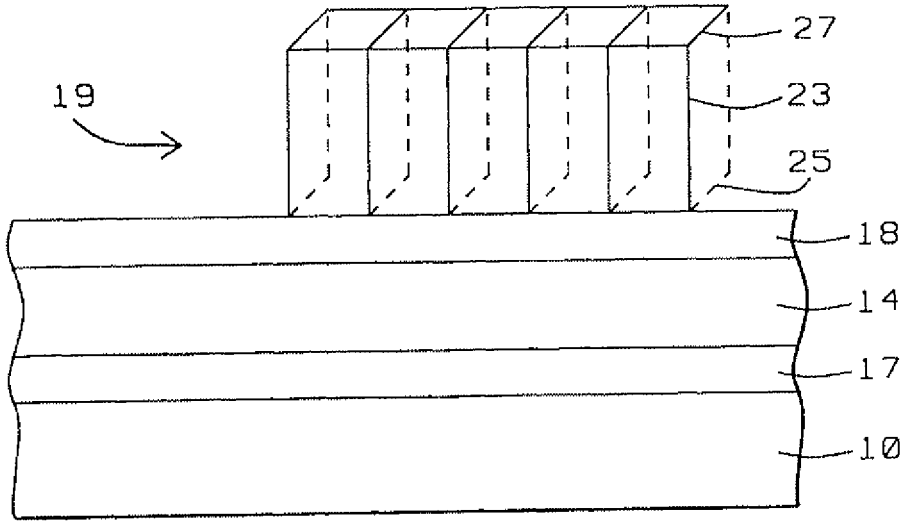

FIG. 6b

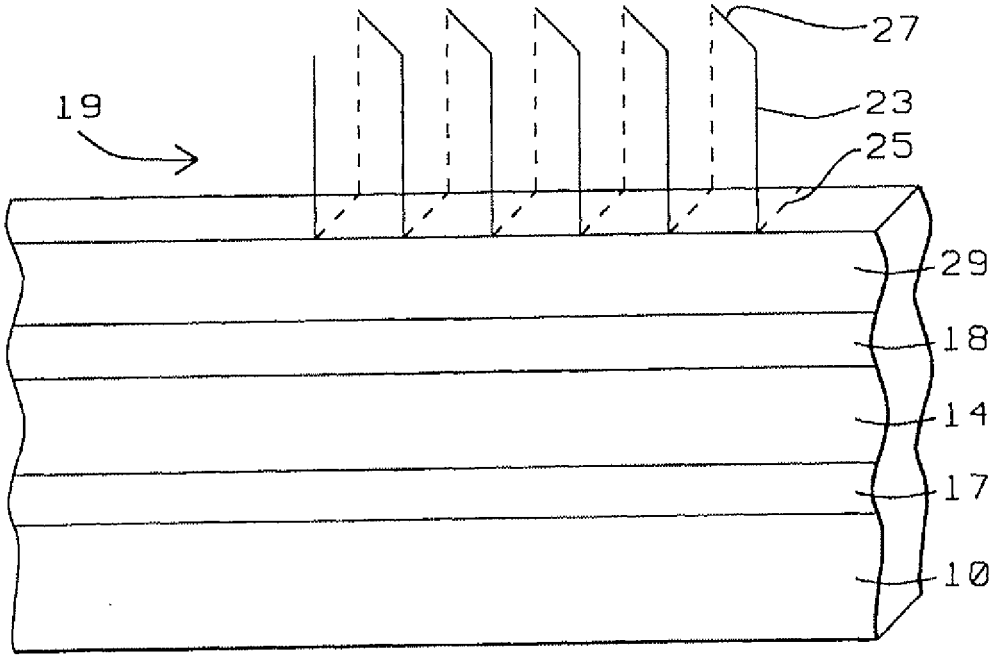

FIG. 6c

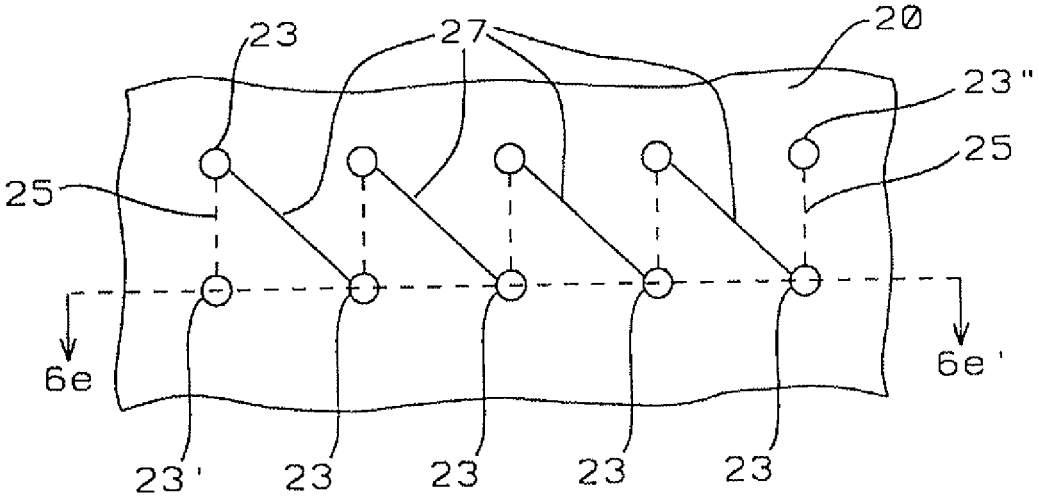

FIG. 6d

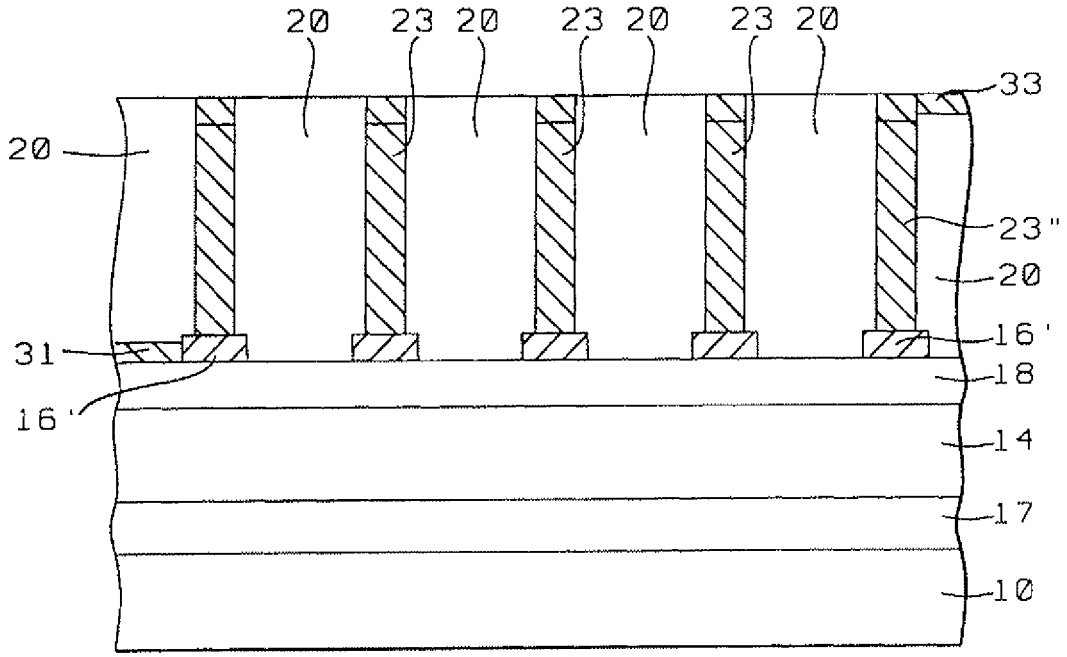
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FIG. 6e

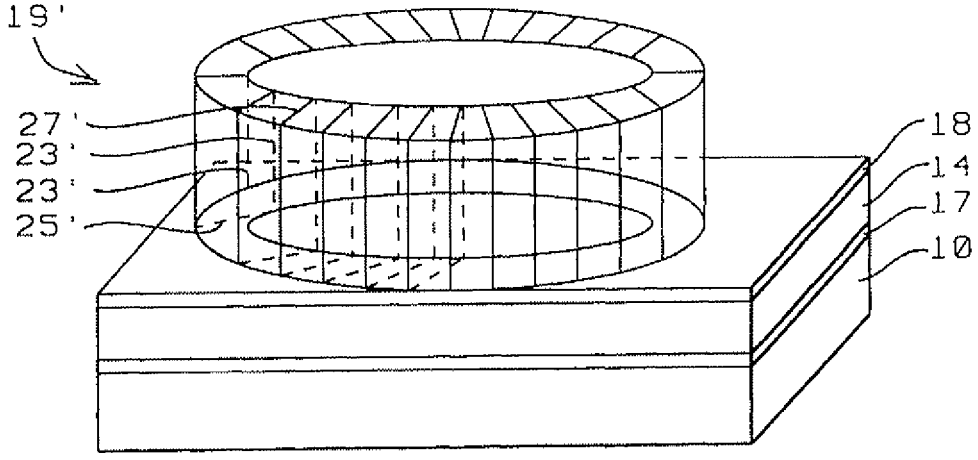
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FIG. 6f

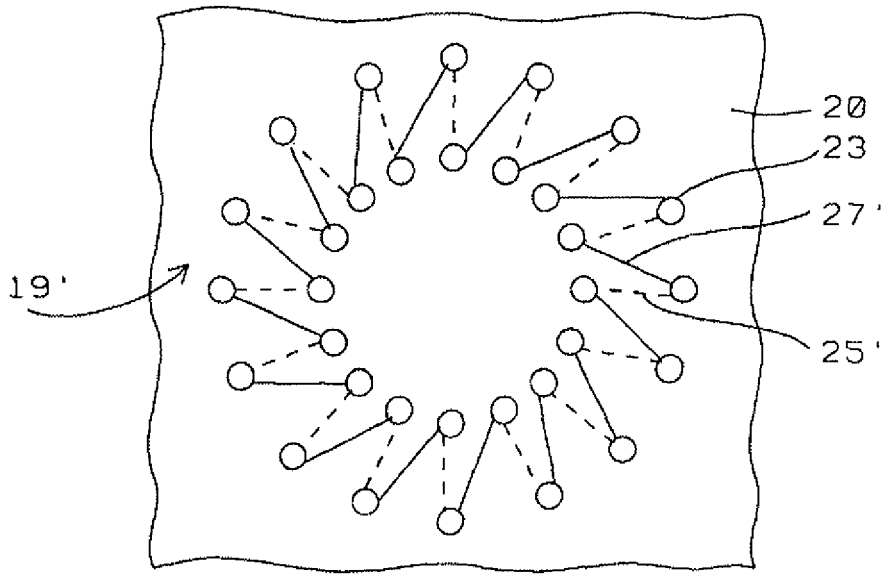

FIG. 6g

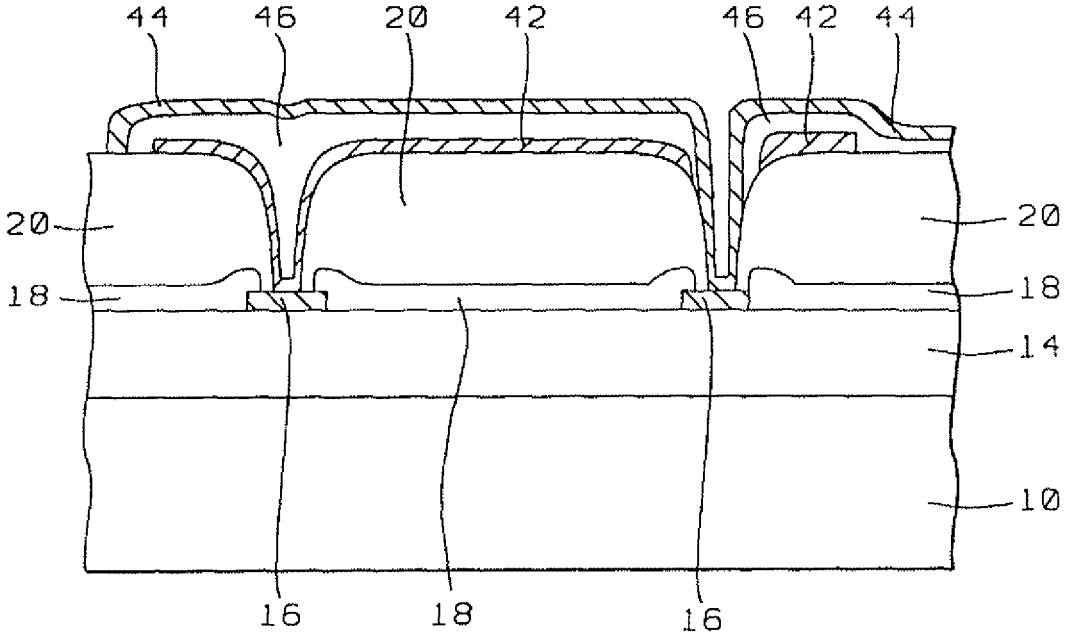

FIG. 7

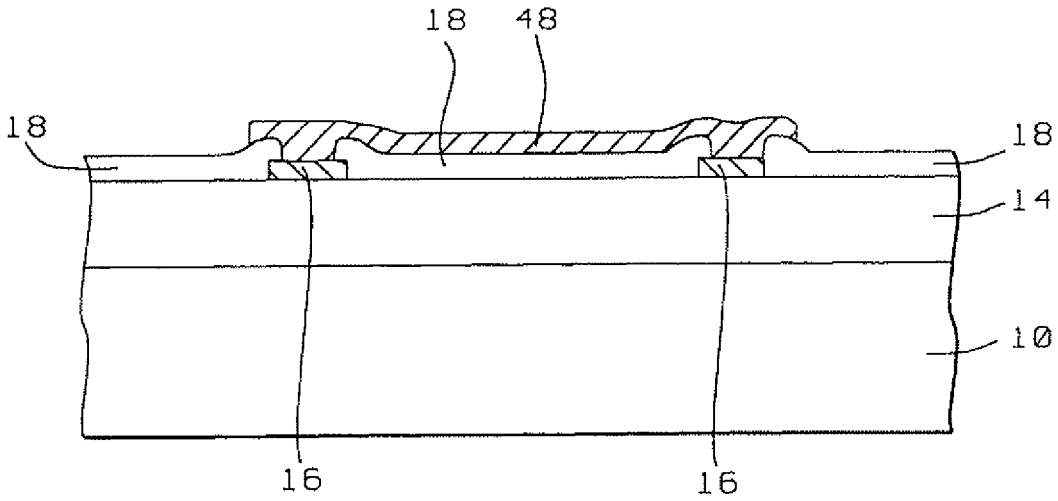

FIG. 8

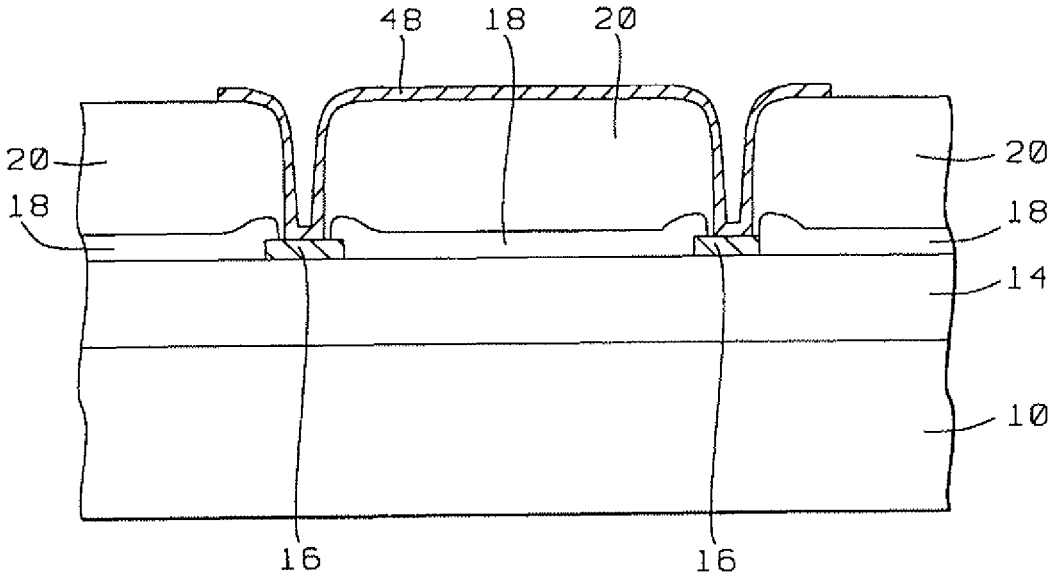

FIG. 9

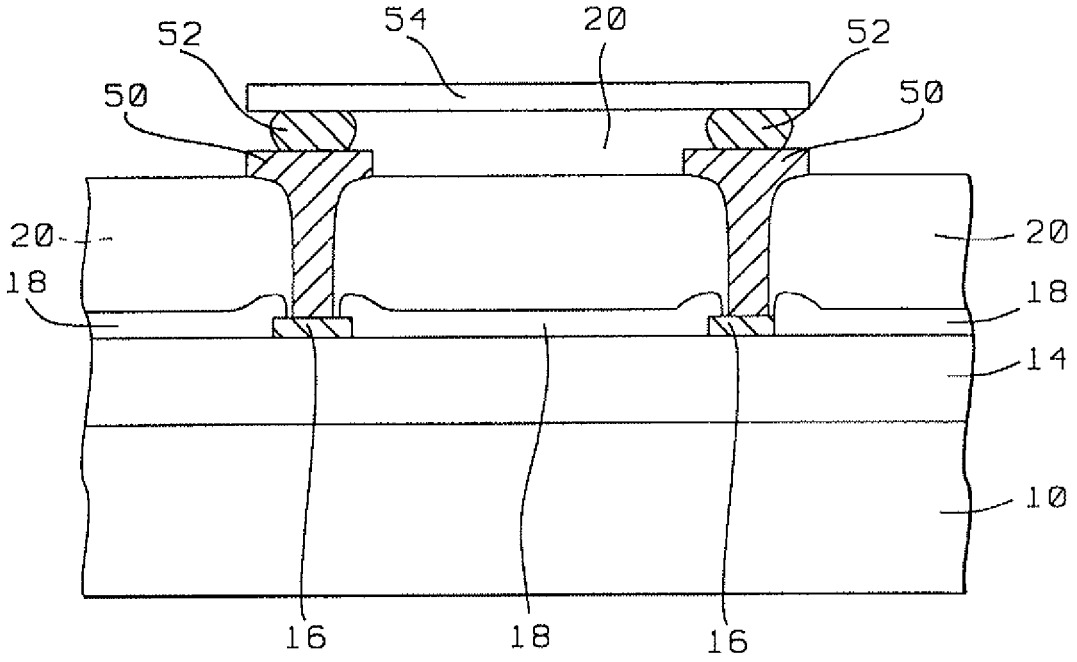
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FIG. 10

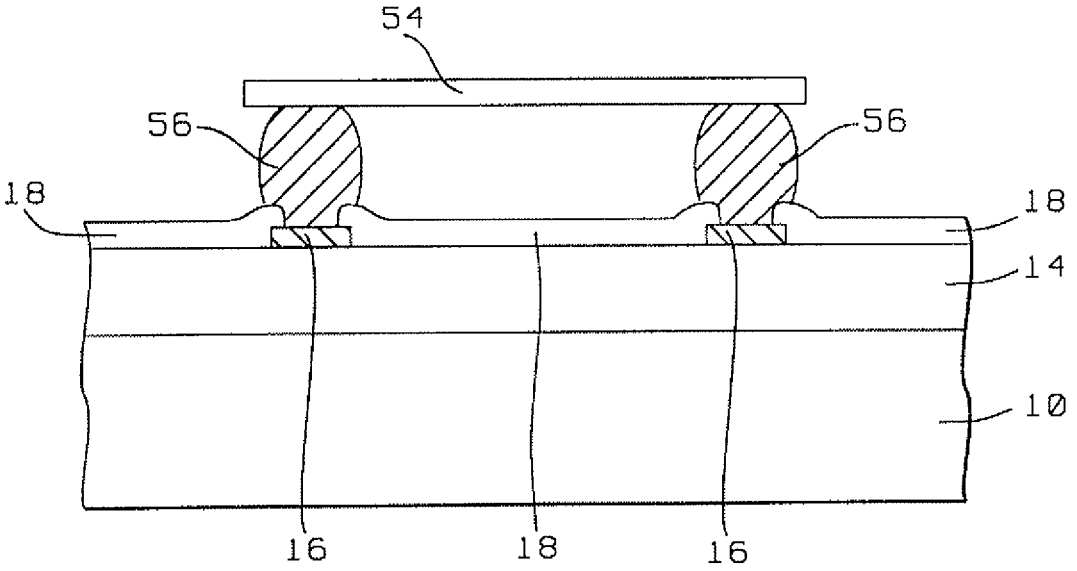
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FIG. 11

HIGH PERFORMANCE SYSTEM-ON-CHIP USING POST PASSIVATION PROCESS

This is a division of patent application Ser. No. 09/970,005, filing date Oct. 3, 2001, High Performance System On-Chip Post Passivation Process, assigned to the same assignee as the present invention of attorney docket MEG00-008, Ser. No. 09/970,005 filing date Oct. 3, 2001, which is a continuation-in-part of attorney docket MSLIN98-002C, Ser. No. 09/251,183, filing date Feb. 17, 1999, which is a continuation-in-part of attorney docket MSLIN98-002, Ser. No. 09/216,791, filing date Dec. 21, 1998 assigned to common assignee.

BACKGROUND OF THE INVENTION

(1) Field of the Invention

The invention relates to the manufacturing of high performance Integrated Circuit (IC's), and, more specifically, to methods of creating high performance electrical components (such as an inductor) on the surface of a semiconductor substrate by reducing the electromagnetic losses that are typically incurred in the surface of the substrate.

(2) Description of the Prior Art

The continued emphasis in the semiconductor technology is to create improved performance semiconductor devices at competitive prices. This emphasis over the years has resulted in extreme miniaturization of semiconductor devices, made possible by continued advances of semiconductor processes and materials in combination with new and sophisticated device designs. Most of the semiconductor devices that are at this time being created are aimed at processing digital data. There are however also numerous semiconductor designs that are aimed at incorporating analog functions into devices that simultaneously process digital and analog data, or devices that can be used for the processing of only analog data. One of the major challenges in the creation of analog processing circuitry (using digital processing procedures and equipment) is that a number of the components that are used for analog circuitry are large in size and are therefore not readily integrated into devices that typically have feature sizes that approach the submicron range. The main components that offer a challenge in this respect are capacitors and inductors, since both these components are, for typical analog processing circuits, of considerable size.

A typical application for inductors of the invention is in the field of modern mobile communication applications that make use of compact, high-frequency equipment. Continued improvements in the performance characteristics of this equipment has over the years been achieved, further improvements will place continued emphasis on lowering the power consumption of the equipment, on reducing the size of the equipment, on increasing the operational frequency of the applications and on creating low noise levels. One of the main applications of semiconductor devices in the field of mobile communication is the creation of Radio Frequency (RE) amplifiers. RE amplifiers contain a number of standard components, a major component of a typical RF amplifier is a tuned circuit that contains inductive and capacitive components. Tuned circuits form, dependent on and determined by the values of their inductive and capacitive components, an impedance that Is frequency dependent, enabling the tuned circuit to either present a high or a low impedance for signals of a certain frequency. The tuned circuit can therefore either reject or pass and further amplify components of an analog signal, based on the frequency of

that component. The tuned circuit can in this manner be used as a filter to filter out or remove signals of certain frequencies or to remove noise from a circuit configuration that is aimed at processing analog signals. The tuned circuit can also be used to form a high electrical impedance by using the LC resonance of the circuit and to thereby counteract the effects of parasitic capacitances that are part of a circuit. One of the problems that is encountered when creating an inductor on the surface of a semiconductor substrate is that the self-resonance that is caused by the parasitic capacitance between the (spiral) inductor and the underlying substrate will limit the use of the inductor at high frequencies. As part of the design of such an inductor it is therefore of importance to reduce the capacitive coupling between the created inductor and the underlying substrate.

At high frequencies, the electromagnetic field that is generated by the inductor induces eddy currents in the underlying silicon substrate. Since the silicon substrate is a resistive conductor, the eddy currents will consume electromagnetic energy resulting in significant energy loss, resulting in a low Q capacitor. This is the main reason for a low Q value of a capacitor, whereby the resonant frequency of $1/\sqrt{(LC)}$ limits the upper boundary of the frequency. In addition, the eddy currents that are induced by the inductor will interfere with the performance of circuitry that is in close physical proximity to the capacitor.

It has already been pointed out that one of the key components that are used in creating high frequency analog semiconductor devices is the inductor that forms part of an LC resonance circuit. In view or the high device density that is typically encountered in semiconductor devices and the therefrom following intense use of the substrate surface area, the creation of the inductor must incorporate the minimization of the surface area that is required for the inductor, while at the same time maintaining a high Q value for the inductor. Typically, inductors that are created on the surface of a substrate are of a spiral shape whereby the spiral is created in a plane that is parallel with the plane of the surface of the substrate. Conventional methods that are used to create the inductor on the surface of a substrate suffer several limitations. Most high Q inductors form part of a hybrid device configuration or of Monolithic Microwave Integrated Circuits (MMIC's) or are created as discrete components, the creation of which is not readily integratable into a typical process of Integrated Circuit manufacturing. It is clear that, by combining the creation on one semiconductor monolithic substrate of circuitry that is aimed at the functions of analog data manipulation and analog data storage with the functions of digital data manipulation and digital data storage, a number of significant advantages can be achieved. Such advantages include the reduction of manufacturing costs and the reduction of power consumption by the combined functions. The spiral form of the inductor that is created on the surface of a semiconductor substrate however results, due to the physical size of the inductor, in parasitic capacitances between the inductor wiring and the underlying substrate and causes electromagnetic energy losses in the underlying resistive silicon substrate. These parasitic capacitances have a serious negative effect on the functionality of the created LC circuit by sharply reducing the frequency of resonance of the tuned circuit of the application. More seriously, the inductor generated electromagnetic field will induce eddy currents in the underlying resistive silicon substrate, causing a significant energy loss that results in low Q inductors.

The performance parameter of an inductor is typically indicated is the Quality (Q) factor of the inductor. The quality factor Q of an inductor is defined as Q=Es/El,

wherein Es is the energy that is stored in the reactive portion of the component while El is the energy that is lost in the reactive portion of the component. The higher the quality of the component, the closer the resistive value of the component approaches zero while the Q factor of the component approaches infinity. For inductors that are created overlying a silicon substrate, the electromagnetic energy that is created by the inductor will primarily be lost in the resistive silicon of the underlying substrate and in the metal lines that are created to form the inductor. The quality factor for components differs from the quality that is associated with filters or resonators. For components, the quality factor serves as a measure of the purity of the reactance (or the susceptance) of the component, which can be degraded due to the resistive silicon substrate, the resistance of the metal lines and dielectric losses. In an actual configuration, there are always some physical resistors that will dissipate power, thereby decreasing the power that can be recovered. The quality factor Q is dimensionless. A Q value of greater than 100 is considered very high for discrete inductors that are mounted on the surface of Printed Circuit Boards. For inductors that form part of an integrated circuit, the Q value is typically in the range between about 3 and 10.

In creating an inductor on a monolithic substrate on which additional semiconductor devices are created, the parasitic capacitances that occur as part of this creation limit the upper bound of the cut-off frequency that can be achieved for the inductor using conventional silicon processes. This limitation is, for many applications, not acceptable. Dependent on the frequency at which the LC circuit is designed to resonate, significantly larger values of quality factor, such as for instance 50 or more, must be available. Prior Art has in this been limited to creating values of higher quality factors as separate units, and in integrating these separate units with the surrounding device functions. This negates the advantages that can be obtained when using the monolithic construction of creating both the inductor and the surrounding devices on one and the same semiconductor substrate. The non-monolithic approach also has the disadvantage that additional wiring is required to interconnect the subcomponents of the assembly, thereby again introducing additional parasitic capacitances and resistive losses over the interconnecting wiring network. For many of the applications of a RF amplifier, such as portable battery powered applications, power consumption is at a premium and must therefore be as low as possible. By raising the power consumption, the effects of parasitic capacitances and resistive power loss can be partially compensated, but there are limitations to even this approach. These problems take on even greater urgency with the rapid expansion of wireless applications, such as portable telephones and the like. Wireless communication is a rapidly expanding market, where the integration of RF integrated circuits is one of the most important challenges. One of the approaches is to significantly increase the frequency of operation to for instance the range of 10 to 100 GHz. For such high frequencies, the value of the quality factor obtained from silicon-based inductors is significantly degraded. For applications in this frequency range, monolithic inductors have been researched using other than silicon as the base for the creation of the inductors. Such monolithic inductors have for instance been created using sapphire or GaAs as a base. These inductors have considerably lower substrate losses than their silicon counterparts (no eddy current, hence no loss of electromagnetic energy) and therefore provide much higher Q inductors. Furthermore, they have lower parasitic capacitance and therefore provide higher frequency operation capabilities. Where however more complex applications are required, the need still exists to create inductors using silicon as a substrate. For those applications, the approach of using a base material other than silicon has proven to be too cumbersome while for instance GaAs as a medium for the creation of semiconductor devices is as yet a technical challenge that needs to be addressed. It is known that GaAs is a semi-insulating material at high frequencies, reducing the electromagnetic losses that are incurred in the surface of the GaAs substrate, thereby increasing the Q value of the inductor created on the GaAs surface. GaAs RF chips however are expensive, a process that can avoid the use of GaAs RF chips therefore offers the benefit of cost advantage.

A number of different approaches have been used to incorporate inductors into a semiconductor environment without sacrificing device performance due to substrate losses. One of these approaches has been to selectively remove (by etching) the silicon underneath the inductor (using methods of micro machining), thereby removing substrate resistive energy losses and parasitic effects. Another method has been to use multiple layers of metal (such as aluminum) interconnects or of copper damascene interconnects.

Other approaches have used a high resistivity silicon substrate thereby reducing resistive losses in the silicon substrate. Resistive substrate losses in the surface of the underlying substrate form a dominant factor in determining the Q value of silicon inductors. Further, biased wells have been proposed underneath a spiral conductor, this again aimed at reducing inductive losses in the surface of the substrate. A more complex approach has been to create an active inductive component that simulates the electrical properties of an inductor as it is applied in active circuitry. This latter approach however results in high power consumption by the simulated inductor and in noise performance that is unacceptable for low power, high frequency applications. All of these approaches have as common objectives to enhance the quality (Q) value of the inductor and to reduce the surface area that is required for the creation of the inductor. The most important consideration in this respect is the electromagnetic energy losses due to the electromagnetic induced eddy currents in the silicon substrate.

When the dimensions of Integrated Circuits are scaled down, the cost per die is decreased while some aspects of performance are improved. The metal connections which connect the Integrated Circuit to other circuit or system components become of relative more importance and have, with the further miniaturization of the IC, an increasingly negative impact on circuit performance. The parasitic capacitance and resistance of the metal interconnections increase, which degrades the chip performance significantly. Of most concern in this respect is the voltage drop along the power and ground buses and the RC delay of the critical signal paths. Attempts to reduce the resistance by using wider metal lines result in higher capacitance of these wires.

Current techniques for building an inductor on the surface of a semiconductor substrate use fine-line techniques whereby the inductor is created under a layer of passivation. This however implies close physical proximity between the created inductor and the surface of the substrate over which the inductor has been created (typically less than 10 μm), resulting in high electro-magnetic losses in the silicon substrate which in turn results in reducing the Q value of the inductor. By increasing the distance between the inductor and the semiconductor surface, the electromagnetic field in the silicon substrate will be reduced in reverse proportion to

the distance, the Q value of the inductor can be increased. By therefore creating the inductor overlying the layer of passivation (by a post passivation process) and by, in addition, creating the inductor on the surface of a thick layer of dielectric (such as a polymer) that is deposited or adhered over the surface of a layer of passivation, the Q value of the inductor can be increased. In addition, by using wide and thick metal for the creation of the inductor, the parasitic resistance is reduced. The process of the invention applies these principles of post passivation inductor creation while the inductor is created on a thick layer of dielectric, using thick and wide metals.

U.S. Pat. No. 5,212,403 (Nakanishi) shows a method of forming wiring connections both inside and outside (in a wiring substrate over the chip) for a logic circuit depending on the length of the wire connections.

U.S. Pat. No. 5,501,006 (Gehman, Jr. et al.) shows a structure with an insulating layer between the integrated circuit (IC) and the wiring substrate. A distribution lead connects the bonding pads of the IC to the bonding pads of the substrate.

U.S. Pat. No. 5,055,907(Jacobs) discloses an extended integration semiconductor structure that allows manufacturers to integrate circuitry beyond the chip boundaries by forming a thin film multi-layer wiring decal on the support substrate and over the chip. However, this reference differs from the invention.

U.S. Pat. No. 5,106,461 (Volfson et al.) teaches a multi layer interconnect structure of alternating polyimide (dielectric) and metal layers over an IC in a TAB structure.

U.S. Pat. No. 5,635,767 (Wenzel et al.) teaches a method for reducing RC delay by a PBGA that separates multiple metal layers.

U.S. Pat. No. 5,686,764 (Fulcher) shows a flip chip substrate that reduces RC delay by separating the power and I/O traces.

U.S. Pat. No. 6,008,102 (Alford et al.) shows a helix inductor using two metal layers connected by vias.

U.S. Pat. No. 5,372,967 (Sundaram et al.) discloses a helix inductor.

U.S. Pat. No. 5'576,680 (Ling) and U.S. Pat. No. 5,884,990 (Burghartz et al.) show other helix' inductor designs.

SUMMARY OF THE INVENTION

It is the primary objective of the invention to improve the RF performance of High Performance Integrated Circuits.

Another objective of the invention is to provide a method for the creation of a high-Q inductor.

Another objective of the invention is to replace the GaAs chip with a silicon chip as a base on which a high-Q inductor is created.

Yet another objective of the invention is to extend the frequency range of the inductor that is created on the surface of a silicon substrate.

It is yet another objective of the invention to create high quality passive electrical components overlying the surface of a silicon substrate.

The above referenced continuation-in-part application adds, in a post passivation processing sequence, a thick layer of dielectric over a layer of passivation and layers of wide and thick metal lines on top of the thick layer of dielectric. The present invention extends the above referenced continuation-in-part application by in addition creating high quality electrical components, such as an inductor, a capacitor or a resistor, on a layer of passivation or on the surface of a thick layer of dielectric. In addition, the process of the invention provides a method for mounting discrete passive electrical components at a significant distance removed from the underlying silicon surface.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** shows a cross section of the interconnection scheme of the referenced continuation-in-part application invention.

FIG. **2** shows a cross section of an extension of the referenced continuation-in-part application whereby an inductor has been created on the surface of a thick layer of polyimide.

FIG. **3** shows a top view of an inductor that is created following the process of the invention.

FIG. **4** shows a cross section of a substrate and overlying layers, an inductor has been created on the surface of a thick layer of polyimide, a layer of ferromagnetic material has been added to further insulate the inductor from the underlying silicon substrate.

FIG. **5***a* shows a cross section of a simplified version of the substrate and the layers that are created on the surface of the substrate using the processes of the referenced continuation-in-part application.

FIG. **5***b* shows the cross section of FIG. **5***a*, an inductor has been added above the layer of passivation.

FIG. **6***a* shows a cross section of a substrate on the surface of which has been deposited a layer of passivation, a capacitor has been created on the surface of the layer of passivation.

FIG. **6***b* shows a three dimensional view of an inductor that has been created on the surface of a layer of passivation by creating vias in a thick layer of polymer.

FIG. **6***c* shows a three-dimensional view of an inductor that has been created in a thick layer of polymer that has been deposited on the surface of a thick layer of polyimide.

FIG. **6***d* shows a top view of the layer **20** on the surface of which an inductor has been created.

FIG. **6***e* shows a cross section of the structure of FIG. **6***d* taken along the line **6***e*–**6***e*' of FIG. **6***d*.

FIG. **6***f* shows a three dimensional view of an inductor that has been created on the surface of a layer of passivation, the Phi inductor has the shape of a solenoid.

FIG. **6***g* shows a top view of the inductor of FIG. **6***f*.

FIG. **7** shows a cross section of a substrate on the surface of which has been deposited a layer of passivation over which a thick layer of polyimide has been deposited, a capacitor has been created on the surface of the thick layer of polyimide.

FIG. **8** shows a cross section of a substrate on the surface of which has been deposited a layer of passivation, a resistor has been created on the surface of the layer of passivation.

FIG. **9** shows a cross section of a substrate on the surface of which has been deposited a layer of passivation over which a thick layer of polyimide has been deposited, a resistor has been created on the surface of the thick layer of polyimide.

FIG. **10** shows a cross section of a silicon substrate on the surface of which a discrete electrical component has been mounted, contact balls are used whereby the distance between the substrate and the electrical component is of a significant value, a thick layer of polyimide has been used.

FIG. **11** shows a cross section of a silicon substrate on the surface of which a discrete electrical component has been

mounted, thick contact balls are used whereby the distance between the substrate and,the electrical component is of a significant value, no layer of polyimide has been used.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The referenced continuation-in-part application teaches an Integrated Circuit structure where re-distribution and interconnect metal layers are created in layers of dielectric on the surface of a conventional IC. A layer of passivation is deposited over the dielectric of the re-distribution and interconnection metal layers, a thick layer of polymer is deposited over the surface of the layer of passivation. Under the present invention, a high-quality electrical component is created on the surface of the thick layer of polymer.

The invention addresses, among others, the creation of an inductor whereby the emphasis is on creating an inductor of high Q value on the surface of a semiconductor substrate using methods and procedures that are well known in the art for the creation of semiconductor devices. The high quality of the inductor of the invention allows for the use of this inductor in high frequency applications while incurring minimum loss of power. The invention further addresses the creation of a capacitor and a resistor on the surface of a silicon substrate whereby the main objective (of the process of creating a capacitor and resistor) is to reduce parasitics that are typically incurred by these components in the underlying silicon substrate.

Referring now more specifically to FIG. **1**, there is shown a cross section of one implementation of the referenced application. The surface of silicon substrate **10** has been provided with transistors and other devices (not shown in FIG. **1**). The surface of substrate **10** is covered by a dielectric layer **12**, layer **12** of dielectric is therefore deposited over the devices that have been provided in the surface of the substrate and over the substrate **10**. Conductive interconnect lines **11** are provided inside layer **12** that connect to the semiconductor devices that have been provided in the surface of substrate **10**.

Layers **14** (two examples are shown) represent all of the metal layers and dielectric layers that are typically created on top of the dielectric layer **12**, layers **14** that are shown in FIG. **1** may therefore contain multiple layers of dielectric or insulation and the like, conductive interconnect lines **13** make up the network of electrical connections that are created throughout layers **14**. Overlying and on the surface of layers **14** are points **16** of electrical contact. These points **16** of electrical contact can for instance be bond pads that establish the electrical interconnects to the transistors and other devices that have been provided in the surface of the substrate **10**. These points of contact **16** are points of interconnect within the IC arrangement that need to be further connected to surrounding circuitry. A passivation layer **18**, formed of for example silicon nitride, is deposited over the surface of layers **14** to protect underlying layers from moisture, contamination, etc.

The key steps of the above referenced application begin with the deposition of a thick layer **20** of polyimide that is deposited over the surface of layer **18**. Access must be provided to points of electrical contact **16**, for this reason a pattern of openings **22**, **36** and **38** is etched through the polyimide layer **20** and the passivation layer **18**, the pattern o. openings **22**, **36** and **38** aligns with the pattern of electrical contact points **16**. Contact points **16** are, by means of the openings **22/36/38** that are created in the layer **20** of polyimide, electrically extended to the surface of layer **20**.

The above referenced material that is used for the deposition of layer **20** is polyimide, the material that can be used for this layer is not limited to polyimide but can contain any of the known polymers, ($SiCl_xO_y$). The indicated polyimide is the preferred material to be used for the processes of the invention for the thick layer **20** of polymer. Examples of polymers that can be used are silicons, carbons, fluoride, chlorides, oxygens, parylene or teflon, polycarbonate (PC), polysterene (PS), polyoxide (PO), poly polooxide (PPO), benzocyclobutene (BCB).

Electrical contact with the contact points **16** can now be established by filling the openings **22/36/38** with a conductive material. The top surfaces **24** of these metal conductors that are contained in openings **22/36/38** can now be used for connection of the IC to its environment, and for further integration into the surrounding electrical circuitry. This latter statement is the same as saying that semiconductor devices that have been provided in the surface of substrate **10** can, via the conductive interconnects contained in openings **22/36/38**, be further connected to surrounding components and circuitry. Interconnect pads **26** and **28** are formed on top of surfaces **24** of the metal interconnects contained in openings **22**, **36** and **38**. These pads **26** and **28** can be of any design in width and thickness to accommodate specific circuit design requirements. A pad can, for instance, be used as a flip chip pad. Other pads can be used for power distribution or as a ground or signal bus. The following connections can, for instance, be made to the pads shown in FIG. 1: pad **26** can serve as a flip chip pad, pad **28** can serve as a flip chip pad or can be connected to electrical power or to electrical ground or to an electrical signal bus. There is no relation between the size of the pads shown in FIG. **1** and the suggested possible electrical connections for which this pad can be used. Pad size and the standard rules and restrictions of electrical circuit design determine the electrical connections to which a giver pad lends itself.

The following comments relate to the size and the number of the contact points **16**, FIG. **1**. Because these contact points **16** are located on top of a thin dielectric (layers **14**, FIG. 1) the pad size cannot be too large since a large pad size brings with it a large capacitance. In addition, a large pad size will interfere with the routing capability of that layer of metal. It is therefore preferred to keep the size of the pad **16** relatively small. The size of pad **16** is however also directly related with the aspect ratio of vias **22/36/38**. An aspect ratio of about 5 is acceptable for the consideration of via etching and via filling. Based on these considerations, the size of the contact pad **16** can be in the order of 0.5 μm to 30 μm, the exact size being dependent on the thickness of layers **18** and **20**.

The referenced application does not impose a limitation on the number of contact pads that can be included in the design, this number is dependent on package design requirements. Layer **18** in FIG. **1** can be a typical IC passivation layer.

The most frequently used passivation layer in the present state of the art is plasma enhanced CVD (PECVD) oxide and nitride. In creating layer **18** of passivation, a layer of approximately 0.2 μm PECVD oxide can be deposited first followed by a layer of approximately 0.7 μm nitride. Passivation layer **18** is very important because it protects the device wafer from moisture and foreign ion contamination. The positioning of this layer between the sub-micron process (of the integrated circuit) and the tens-micron process (of the interconnecting metalization structure) is of critical importance since it allows for a cheaper process-that possibly has less stringent clean room requirements for the process of creating the interconnecting metalization structure.

Layer **20** is a thick polymer dielectric layer (for example polyimide) that have a thickness in excess of 2 μm (after curing). The range of the polymer thickness can vary from 2 μm to 150 μm, dependent on electrical design requirements.

For the deposition of layer **20** the Hitachi-Dupont polyimnide HD 2732 or 2734 can, for example, be used. The polyimide can be spin-on coated and cured. After spin-on coating, the polyimide will be cured at 400 degrees C. for about 1 hour in a vacuum or nitrogen ambient. For a thicker layer of polyimide, the polyimide film can be multiple coated and cured.

Another material that can be used to create layer **20** is the polymer benzocyclobutene (BCB). This polymer is at this time commercially produced by for instance Dow Chemical and has recently gained acceptanee to be used instead of typical polyimide application.

The dimensions of openings **22, 36** and **38** have previously been discussed. The dimension of the openings together with the dielectric thickness determine the aspect ratio of the opening. The aspect ratio challenges the via etch process and the metal filling capability. This leads to a diameter for openings **22/36/38** in the range of approximately 0.5 μm to 30 μm, the height for openings **22/36/38** can be in the range. of approximately 2 μm to 150 μm. The aspect ratio of openings **22/36/38** is designed such that filling of the via with metal can be accomplished. The via can be filled with CVD metal such as CVD tungsten or CVD copper, with electro-less nickel, with a damascene metal filling process, with electroplating copper, etc.

The referenced application can be further extended by applying multiple layers of polymer (such as polyimide) and can therefore be adapted to a larger variety of applications. The function of the structure that has been described in FIG. **1** can be further extended by depositing a second layer of polyimide on top of the previously deposited layer **20** and overlaying the pads **26** and **28**. Selective etching and metal deposition can further create additional contact points on the surface of the second layer of polyimide that can be interconnected with pads **26** and **28**. Additional layers of polyimide and the thereon created contact pads can be customized to a particular application, the indicated extension of multiple layers of polyimides greatly enhances the flexibility and usefulness of the referenced continuation-in-part application.

FIG. **1** shows a basic design advantage of the referenced continuation-in-part application. This advantage allows for sub-micron or fine-lines, that rum, in the immediate vicinity of the metal layers **14** and the contact points lo, to be extended in an upward direction **30** through metal interconneet **36**. This extension continues in the direction **32** in the horizontal plane of the metal interconneet **28** and comes back down in the downward direction **34** through metal interconneet **38**. The functions and constructs of the passivation layer **18** and the insulating layer **20** remain as previously highlighted. This basic design advantage of the invention is to "elevate" or "fan-out" the fine-line interconnects and to remove these interconnects from the micro and sub-micro level to a metal interconneet level that has considerably larger dimensions and that therefore has smaller resistance and capacitance and is easier and more cost effective to manufacture. This aspect of the referenced application does not include any aspect of conducting line re-distribution and therefore has an inherent quality of simplicity. It therefore further adds to the importance of the referenced application in that it makes micro and sub-micro wiring accessible at a wide and thick metal level. The interconnections **20, 36** and **38** interconneet the fine-level metal by going up through the passivation and polymer or polyimide dielectric layers, continuing over a distance on the wide and thick metal level and continuing by descending from the wide and thick metal level back down to the fine-metal level by again passing down through the passivation and polymer or polyimide dielectric layers. The extensions that are in this manner accomplished need not be limited to extending fine-metal interconneet points **16** of any particular type, such as signal or power or ground, with wide and thick metal line **26** and **28**. The laws of physics and electronics will impose limitations, if any, as to what type of interconneet can by established in this manner, limiting factors will be the conventional electrical limiting factors of resistance, propagation delay, RC constants and others. Where the referenced application is of importance is that the referenced continuation-in-part application provides much broader latitude in being able to apply these laws and, in so doing, provides a considerably extended scope of the application and use of Integrated Circuits and the adaptation of these circuits to a wide and thick metal environment.

FIG. **2** shows how the basic interconneet aspect of the referenced continuation-in-part application can further be extended under the present invention to not only elevate the fine-metal to the plane of the wide and thick metal but to also add an inductor on the surface of the thick layer **20** of polyimide. The inductor is created in a plane that is parallel with the surface of the substrate **10** whereby this plane however is separated from the surface of the substrate **10** by the combined heights of layers **12, 14, 18,** and **20**. FIG. **2** shows a cross section **40** of the inductor taken in a plane that is perpendicular to the surface of substrate **10**. The wide and thick metal will also contribute to a reduction of the resistive energy losses. Furthermore, the low resistivity metal, such as gold, silver and copper, can be applied using electroplating, the thickness can be about 20 μm.

FIG. **3** shows a top view **42** of the spiral structure of the inductor **40** that has been created on the surface of layer **20** of dielectric. The cross section that is shown in FIG. **2** of the inductor **40** has been taken along the line **2--2'** of FIG. **3**. The method used for the creation of the inductor **40** uses conventional methods of metal, such as gold, copper and the like, deposition by electroplating or metal sputter processes.

FIG. **4** shows a top view of inductor **40** whereby the inductor has been further isolated from the surface of the substrate **10** by the addition of layer **44** of ferromagnetic material. Openings are created in layer **44** of ferromagnetic material for the conductors **36** and **38**, the layer **44** is deposited using conventional methods to a thickness that can be experimentally determined and that is influenced by and partially dependent on the types of materials used and the thickness of the layers that are used overlying the ferromagnetic material (such as layer **20**) for the creation of the structure that is shown in cross section in FIG. **4**. The surface area of the ferromagnetic layer **44** typically extends over the surface of layer **18** such that the inductor **40** aligns with and overlays the layer **44**, the surface area of layer **44** can be extended slightly beyond these boundaries to further improve shielding the surface of substrate **10** from the electromagnetic field of inductor **40**.

Layer **44** is not limited to being a layer of ferromagnetic material but can also be a layer of a good conductor such as but not limited to gold, copper and aluminum. The overlying inductor **40** that is created on the surface of layer **20** of polyimide can be isolated from the underlying silicon substrate **10** by a layer **44** that comprises either ferromagnetic or a good conductor.

FIG. 5*a* shows, for reasons of clarity, a simplified cross section of the substrate and the layers that are created on the surface of the substrate under the processes of the invention, the highlighted areas that are shown have previously been identified as:

10, the silicon substrate

12, a layer of dielectric that has been deposited over the surface of the substrate

14, an interconnect layer that contains interconnect lines, vias and contact points

16, contact points on the surface of the interconnect layer **14**

18, a layer of passivation into which openings have been created through which the contact points **16** can be accessed

20, a thick layer of polymer, and

21, conductive plugs that have been provided through the layer **20** of polyamide.

The thick layer **20** of polymer can be coated in liquid form on the surface of the layer **18** of passivation or can be laminated over the surface of layer **18** of passivation by dry film application. Vias that are required for the creation of conductive plugs **21** can be defined by conventional processes of photolithography or can be created using laser (drill) technology.

It is clear from previous discussions that the sequence of layers that is shown in cross section in FIG. 5*a* has been created so that additional electrical components such as an inductor, a capacitor and the like can be created on the surface of layer **20** of polyimide and in electrical contact with conductive plugs **21**. Layer **12** of dielectric may, in the cross section that is shown in FIG. 5*a*, be part of layer **14** since layer **14** is a layer of Intra Level Dielectric (ILD) within which layer **12** can be readily integrated.

With respect to the cross section that is shown in FIG. 5*b*, the same layers that have been identified for FIG. 5*a* are again provided in this cross section. Additionally has been shown the upper layer **17** of the silicon substrate **10** that contains active semiconductor devices. Also shown is the cross section of an inductor **19** that has been created on the surface of layer **18** of passivation. It must again be emphasized that the ohmic resistivity of the metal that is used for inductor **19** must be as low as possible. For this reason, the use of a thick layer of for instance gold is preferred for the formation of inductor **19**. It has been shown that a thick layer of gold increased the Q value of inductor **19** from about 5 to about 20 for 2.4 GHz applications, which represents a significant improvement in the Q value of inductor **19**.

FIG. 6*a* shows a cross section of a capacitor that has been created on the surface of a substrate **10**. A layer **14** of conductive interconnect lines and contact points has been created on the surface of substrate **10**. A layer **18** of passivation has been deposited over the surface of layer **14**, openings have been created in layer **18** of passivation through which the surface of contact pads **16** can be accessed.

A capacitor contains, as is well known, a lower plate, an upper plate and a layer of dielectric that separates the upper plate from the lower plate. These components of a capacitor can be readily identified from the cross section that is shown in FIG. 6*a*, as follows:

42 is a conductive layer that forms the lower plate of the capacitor

44 is a conductive layer that forms the upper plate of the capacitor

46 is the dielectric layer that separates the upper plate **44** of the capacitor from the lower plate **42**.

It must be noted from the cross section that is shown in FIG. 6*a* that the capacitor has been created on the surface of layer **18** of passivation, the process of creating the capacitor is therefore referred to as a post-passivation processing sequence. Processing conditions and materials that can be used for the creation of the respective layers **42**, **44** and **46** have already been highlighted and need therefore not be further detailed at this time.

The main points of interest are the various thicknesses to which the three layers **42**, **44** and **46** can be deposited, as follows:

layer **18** of passivation between about 0.1 μm and 0.3 μm

layer **42** of conductive material between about 0.5 and 20 μm

layer **44** of dielectric between about 500 and 10,000 Angstrom, and

layer **46** of conductive material between about 0.5 and 20 μm.

The post-passivation created capacitor that is shown in cross section in FIG. 6*a* has:

reduced parasitic capacitance between the capacitor and the underlying silicon substrate

allowed for the use of a thick layer of conductive material, reducing the resistance of the capacitor; this is particularly important for wireless applications

allowed for the use of high-dielectric material such as TiO_2, Ta_2O_5 for the dielectric between the upper and the lower plate of the capacitor, resulting in a higher capacitive value of the capacitor.

FIG. 6*b* shows a three-dimensional view of the solenoid structure of an inductor **19** that has been created on the surface of the layer **18** of passivation. Further highlighted in FIG. 6*b* are:

23, vias that are created in the thick layer of polymer **20**, FIG. 5*a*, for the interconnects of the upper and the lower levels of metal of the inductor

25, the bottom metal of the inductor

27, the top metal for the inductor.

FIG. 6*c* shows a three dimensional view of an inductor that has been created on the surface of a layer **18** of passivation by first depositing a thick layer **29** of polymer over which a layer (not shown) of polymer is deposited, vias **23** are created in the thick layer **20** (FIG. 5*a*) of polymer. In addition to the previously highlighted layers, FIG. 6*c* shows a layer **29** of polyimide. The inductor **19** is created by creating the bottom metal **25** of the inductor **19**, the top metal **27** of the inductor and the vias **23** that are created in layer **20** (FIG. 5*a*) that preferably contains a polymer.

FIG. 6*d* shows a top view of layer **20** on the surface of which an inductor has been created as previously shown in FIG. 6*c*. Vias **23** are highlighted as are top metal lines **27** of the inductor **19**, bottom metal lines **25** of the inductor **19** (hatched since they are not visible on the surface of the layer **20**). Further detailed are vias **23'** and **23"**, the lower extremity of via **23'** and the upper extremity of via **23"** are connected to interconnect lines **31** and **33** (FIG. 6*e*) respectively, theses interconnect lines **31** and **33** provide the connection for further interconnect of the inductor **19**.

FIG. 6*e* shows a cross section of the structure of FIG. 6*d* whereby this cross section is taken along the line 6*e*–6*e'* that is shown in FIG. 6*d*. Contact pads **16'** have been provided on the surface of layer **18** of passivation, these contact pads **16'** make contact with the vias **23**, **23'** and **23"** for interconnection between the bottom metal **25** of inductor **19** and the upper metal **27** of the inductor **19**. Interconnects to vias **23'**

and **23"** are the lines **31** and **33** which, as previously stated, connect the inductor **19** to surrounding electrical circuitry or components.

The creation of a toroidal inductor overlying a layer of passivation has been shown in FIGS. **6***f* and **6***g* where toroidal coil **19'** is created on the surface of a layer **18** of passivation. Top level metal **27'**, bottom level metal **25'** and vias **23'** that interconnect bottom level metal **25'** with top level metal **27'** have been highlighted in FIG. **6***f*.

FIG. **6***g* shows, for further clarification, a top view of the toroidal **19'** of FIG. **6***f*. The highlighted features of this figure have previously been explained and therefore do not need to be further discussed at this time.

FIG. **7** shows a cross section where, as in FIG. **6***a*, a capacitor is created on the surface of substrate **10**. In the cross section that is shown in FIG. **7** however a thick layer **20** of polyimide has been deposited over the surface of the passivation layer **18** and has been patterned and etched in order to make the contact pads **16** accessible though the thick layer **20** of poly. The thick layer **20** of polymer removes most of the capacitor, that is the lower plate **42**, the upper plate **44** and the dielectric **46**, from the surface of substrate **10** by a distance that is equal to the thickness of layer **20**. It has previously been state that the range of polyimide thickness can vary from 2 μm to 150 μm and is dependent on electrical design requirements. This statement is also valid for the cross section shown in FIG. **7**, the layers-of the capacitor can therefore be removed from the surface of substrate **10** by a distance of 2 μm to 150 μm. It is clear that this leads to a significant increase in distance between the capacitor and the underlying silicon substrate, the parasitic capacitance will therefore be significantly reduced.

FIG. **8** shows a cross section of a substrate **10** on the surface of which has been deposited a layer **18** of passivation, a resistor **48** has been oreated on the surface of the layer **18** of passivation. A resistor, as is well known, is created by connecting two points with a material that offers electrical resistance to the passage of current through the material. The two points that are part of the resistance **48** that is shown in cross section in FIG. **8** are the contact pads **16** that have been created in or on the surface of the interconnect layer **14**. By creating layer **48** between the two contact pads, that interconnects the two contact pads and that is deposited on the surface of passivation layer **18**, a resistor has been created in accordance with the processes of the invention. For the creation of layer **48** a high resistivity material can be used such as TaN, silicon nitride, phosphosilicate glass (PSG), silicon oxynitride, aluminum, aluminum oxide (Al_xO_y), tantalum, nionbium, or molybdenum. It is clear that dimensions such as thickness, length and width of deposition of layer **48** of high resistivity material are application dependent and can therefore not be specified at this time in any detail. The resistor that is shown in cross section in FIG. **8** is, as are the capacitors of FIGS. **6***a* and **7**, created in a post-passivation process on the surface of layer **18** of passivation.

FIG. **9** shows a cross section of a substrate **10**, an interconnect layer **14** has been created on the surface of the substrate. A layer **18** of passivation has been deposited over the layer **14** of interconnect metal, a thick layer **20** of polyimide has been deposited over the surface of the passivation layer **18**. A resistor **48** has been created on the surface of the layer **20** of polyimide. The resistor **48** is created connecting the two contact pads **16** with a thin high resistivity layer of metal. By increasing the distance between the body of the resistor and the surface of substrate (by the thickness of the poly layer **20**) the parasitic capacitance between the body of the resistor and the substrate is reduced resulting in an improved resistive component (reduced parasitic capacitive loss, improved high frequency performance).

Further applications of the post-passivation processing of the invention are shown in FIGS. **10** and **11**, which concentrate on making ball contact points between contact pads **16** and an overlying electric component, such as a discrete inductor. Proceeding from the surface of substrate **10** in an upward direction, most of the layers that are shown in FIG. **10** have previously been identified and are identified in FIG. **10** using the same numerals as have previously been used for these layers. Where FIG. **10** shows previously not identified layers is in:

- **50**, contact plugs that have been formed through the thick layer **20** of polymer
- **52**, contact balls that,have been formed on the surface of the contact plugs **50** using conventional methods of selective solder deposition (plating or ball mounting on the surface of plugs **50**), the application of a flux on the deposited solder and flowing the solder to form the contact balls **52**, and
- **54**, a cross section of a discrete electrical component such as an inductor or a discrete capacitor or a resistor.

FIG. **11** shows a cross section of a silicon substrate **10** on the surface of which a discrete electrical component **54** has been mounted, contact balls **56** are used whereby the distance between the substrate **10** and the electrical component **54** is of a significant value. Contact balls are inserted into the openings that have been created in the layer **18** of passivation overlying the contact pads **16**, the (relatively large) contact balls **56** create a significant separation between the surface of substrate **10** and the-discrete electrical component **54**.

The methods that have been shown in FIGS. **10** and **11** indicate that:

- the passive component **54** is removed from the surface of substrate **10** by a significant distance, and
- instead of mounting the-passive, discrete component **54** on the surface of a Printed Circuit Board (PCB), the passive component **54** can be mounted closer to a semiconductor device in the present invention.

Throughout the methods and procedures that have been explained above using the examples that are shown in cross section in the accompanying drawings, the following has been adhered to:

- the passive components have been further removed from the silicon substrate, thereby reducing the negative impact that is induced by the substrate due to electromagnetic losses incurred in the substrate
- the post-passivation process of the invention allows for the selection of discrete component design parameters that result in reduced resistance of the discrete capacitor and the discrete inductor, this is further clear from the following comparison between prior art processes and the processes of the invention.

Prior art requires for the creation of an inductor:

the use of thin metal, which imposes the creation of wide coils for an inductor resulting in

increased surface area that is required for the inductor which in turn increases the parasitic capacitance of the inductor causing eddy current losses in the surface of the substrate.

The present invention by contrast:

can use thick metal, since the metal of the passive component is (by the thick layer of polymer) removed from the (thin metal) interconnect layer **14**, and (as a consequence)

reduces the surface area that is required for the inductor, and

reduces the resistivity of the inductor, thereby increasing the Q value of the inductor.

Although the preferred embodiment of the present invention has been illustrated, and that form has been described in detail, it will be readily understood by those skilled in the art that various modifications may be made therein without departing from the spirit of the invention or from the scope of the appended claims.

What is claimed is:

1. A discrete electrical component above the surface of a semiconductor substrate, comprising:

a semiconductor substrate, in or on the surface of which semiconductor devices have been created, having points of electrical contact provided to said semiconductor devices in or on the active surface of said substrate;

an overlaying interconnecting metalization structure comprising one or more layers of interconnects over the active surface of said substrate, said layers of interconnects comprising conductive interconnect lines or conductive contact points or conductive vias in one or more layers, with points of electrical contact having been provided in or on the surface of said overlaying interconnecting metalization structure, at least one of said points of electrical contact making contact with at least one of said conductive interconnect lines or said conductive contact points or said conductive vias provided in said one or more layers of said overlaying interconnecting metalization structure, at least one of said metal lines or said contact points or said conductive vias making contact with at least one of said points of electrical contact provided to said semiconductor devices in or on the surface of said substrate;

a passivation layer deposited over said overlaying interconnecting metalization structure;

openings created in said layer of passivation, at least two of said openings overlaying at least one pair of points of electrical contact having been provided in the surface of said overlaying interconnecting metalization structure, providing at least one pair of points of electrical contact in said layer of passivation;

an polymer insulating, separating layer deposited over the surface of said patterned and etched layer of passivation, including said openings created in said layer of passivation;

at least one pair of openings created in said polymer insulating, separating layer that aligns with at least one pair of points of electrical contact provided in said layer of passivation;

a layer of conductive material selectively deposited over the surface of at least one pair of points of electrical contact provided in said layer of passivation, filling said openings created in said polymer insulating, separating layer, creating conductive plugs through said polymer insulating, separating layer, said conductive plugs overlaying at least one pair of points of electrical contact provided in said layer of passivation;

a layer of solder selectively created over the surface of said conductive plugs;

said discrete electrical component positioned above and in alignment with said selectively created layer of solder such that electrical contact points of said discrete electrical component align with said selectively created layer of solder; and

said selectively created layer of solder flowed, creating solder balls connecting said discrete electrical component with said conductive plugs in said polymer insulating, separating layer, thereby connecting said discrete electrical component with a pair of points of electrical contact in said layer of passivation.

2. The discrete electrical component of claim 1 wherein said passivation layer comprises a layer within the range of approximately 0.15 to 2.0 μm of Plasma Enhanced CVD (PECVD) oxide over which a layer within the range of approximately 0.5 to 2.0 μm PECVD nitride is deposited.

3. The discrete electrical component of claim 1 wherein said polymer insulating, separating layer comprises polyimide or the polymer benzocyclobutene (BCB).

4. The discrete electrical component of claim 1 wherein said polymer insulating, separating layer is of a thickness after curing within the range of approximately 1.0 to 150 μm.

5. The discrete electrical component of claim 1, wherein said polymer insulating, separating layer is spin-on coated and cured.

6. The discrete electrical component of claim 1 Wherein said polymer insulating, separating layer is subjected to multiple processing steps of spin on coating and curing.

7. The discrete electrical component of claim 1 wherein said discrete electrical component is selected from a group comprising a resistor, a capacitor and an inductor.

8. A discrete electrical component mounted above the surface of a semiconductor substrate, comprising:

a semiconductor substrate, in or on the surface of which semiconductor devices have been created, having points of electrical contact provided to said semiconductor devices in or on the active surface of said substrate;

an overlaying interconnecting metalization structure comprising one or more layers of interconnects over the active surface of said substrate, said layers of interconnects comprising conductive interconnect lines or conductive contact points or conductive vias in one or more layers, with points of electrical contact having been provided in or on the surface of said overlaying interconnecting metalization structure, at least one of said points of electrical contact making contact with at least one of said conductive interconnect lines or said conductive contact points or said conductive vias provided in said one or more layers of said overlaying interconnecting metalization structure, at least one of said metal lines or said contact points or said conductive vias making contact with at least one of said points of electrical contact provided to said semiconductor devices in or on the surface of said substrate;

a passivation layer deposited over said overlaying interconnecting metalization structure;

openings created in said layer of passivation, at least two of said openings overlaying at least one pair of points of electrical contact having been provided in the surface of said overlaying interconnecting metalization structure, providing at least one pair of points of electrical contact in said layer of passivation;

a layer of solder selectively deposited over the surface of at least one pair of points of electrical contact in said layer of passivation;

said discrete electrical component positioned above and aligned with said selectively deposited layer of solder such that electrical contact points of said discrete electrical component align with said selectively deposited layer of solder; and

said layer of selectively deposited solder flowed, creating solder balls connecting said discrete electrical component with at least one pair of points of electrical contact in said layer of passivation.

9. The discrete electrical component of claim 8 wherein said passivation layer comprises a layer within the range of approximately 0.15 to 2.0 μm of Plasma Enhanced CVD (PECVD) oxide over which a layer within the range of approximately 0.5 to 2.0 μm PECVD nitride deposited.

10. The discrete electrical component of claim 8 wherein said discrete electrical component is selected from a group comprising a resistor, a capacitor and an inductor.

* * * * *

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[54] **DUAL DAMASCENE PATTERNED CONDUCTOR LAYER FORMATION METHOD WITHOUT ETCH STOP LAYER**

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[51] **Int. Cl.**[6] **H01L 21/30**

[52] **U.S. Cl.** **438/706**; 438/711; 438/723

[58] **Field of Search** 438/706, 711, 438/712, 714, 717, 723, 700, 221, 740

[56] **References Cited**

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5,380,546	1/1995	Krishnan et al.	427/126.1
5,466,639	11/1995	Ireland	437/195
5,565,384	10/1996	Havemann	437/228
5,635,423	6/1997	Huang et al.	437/195
5,686,354	11/1997	Avanzino et al.	437/190
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Korczynski, "Low-K Dielectric Integration Costmodelling" Solid State Technology, Oct. 1997, p. 123–28.

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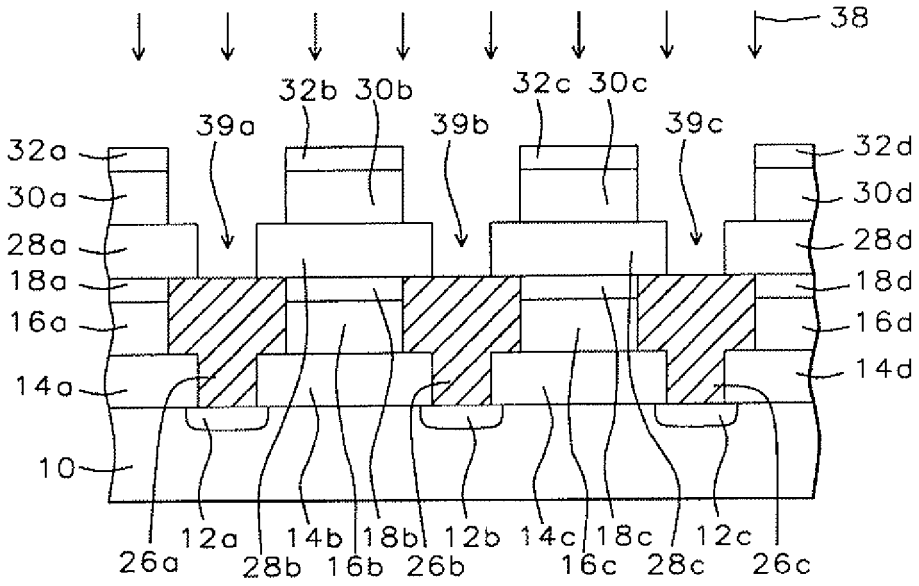
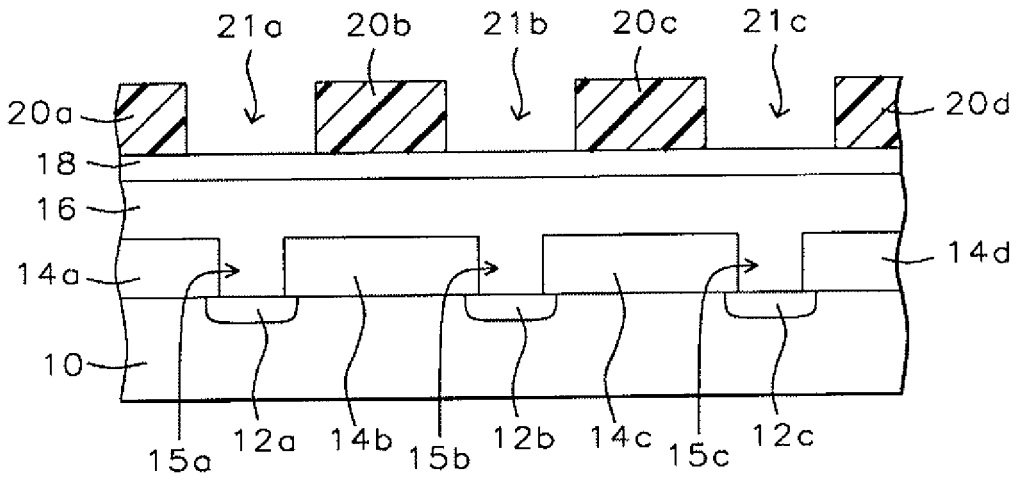
Assistant Examiner—Kin-Chan Chen
Attorney, Agent, or Firm—George O. Saile; Stephen B. Ackerman; Alek P. Szecsy

[57] **ABSTRACT**

A method for forming a via through a dielectric layer within a microelectronics fabrication. There is first provided a substrate employed within a microelectronics fabrication. There is then formed upon the substrate a patterned first dielectric layer which defines a via accessing a contact region formed within the substrate. The patterned first dielectric layer is formed of a first dielectric material which is not susceptible to etching with an oxygen containing plasma. There is then formed upon the patterned first dielectric layer a blanket second dielectric layer which completely covers the patterned first dielectric layer and fills the via. The blanket second dielectric layer is formed of a second dielectric material which is susceptible to etching within the oxygen containing plasma. There is then formed upon the blanket second dielectric layer a blanket hard mask layer which is formed from a hard mask material which is not susceptible to etching within the oxygen containing plasma. There is then formed upon the blanket hard mask layer a patterned photoresist layer which leaves exposed a portion of the blanket hard mask layer greater that an areal dimension of the via and at least partially overlapping the areal dimension of the via. There is then etched while employing a first plasma etch method the blanket hard mask layer to form a patterned hard mask layer defining a first trench formed through the patterned hard mask layer while employing the patterned photoresist layer as a first etch mask layer. The first plasma etch method employs a first etchant gas composition appropriate to the hard mask material from which is formed the blanket hard mask layer. Finally, there is then etched while employing a second plasma etch method the blanket second dielectric layer to form a patterned second dielectric layer having an aperture formed therethrough. The aperture comprises: (1) a second trench corresponding with the first trench; and (2) at least a portion of the first via. The second plasma etch method employs the oxygen containing plasma.

13 Claims, 4 Drawing Sheets

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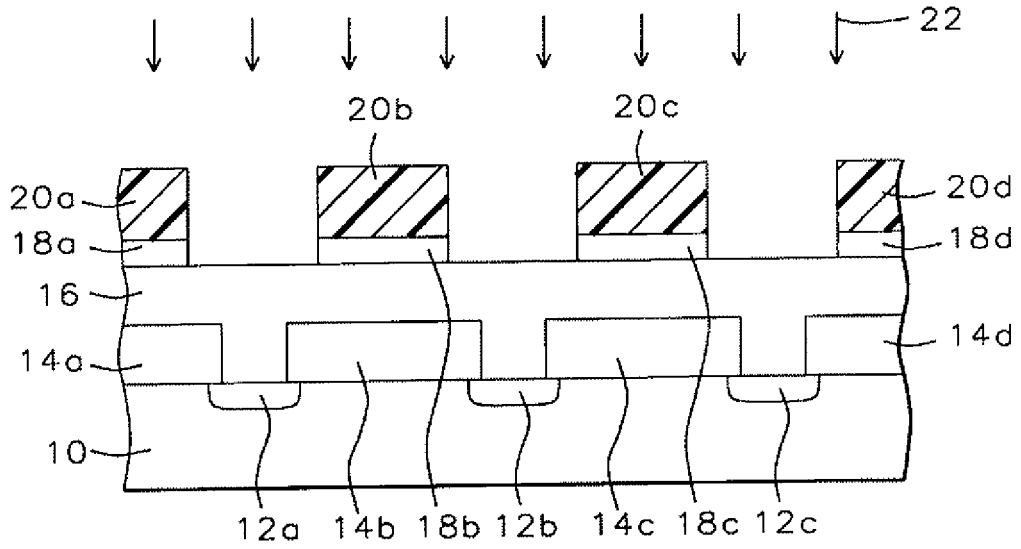
14c
15c
12c

FIG. 1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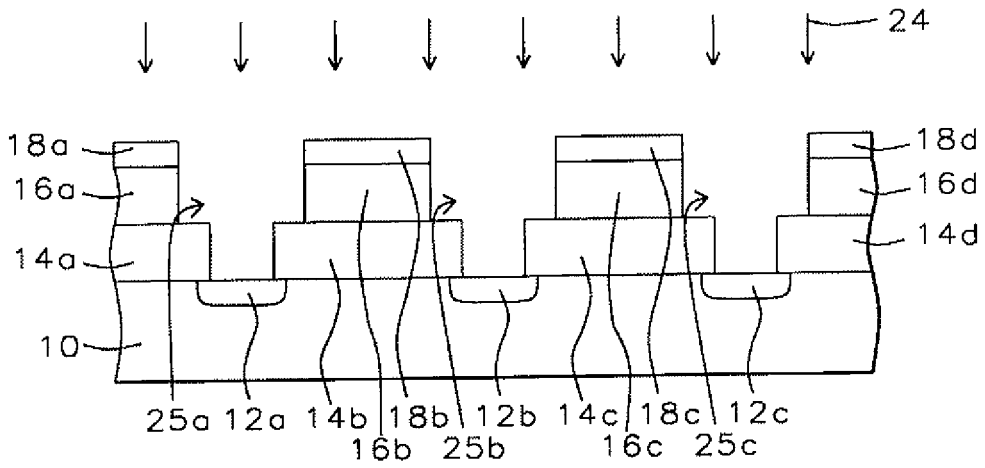
18c
12c

FIG. 2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18a
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10
18d
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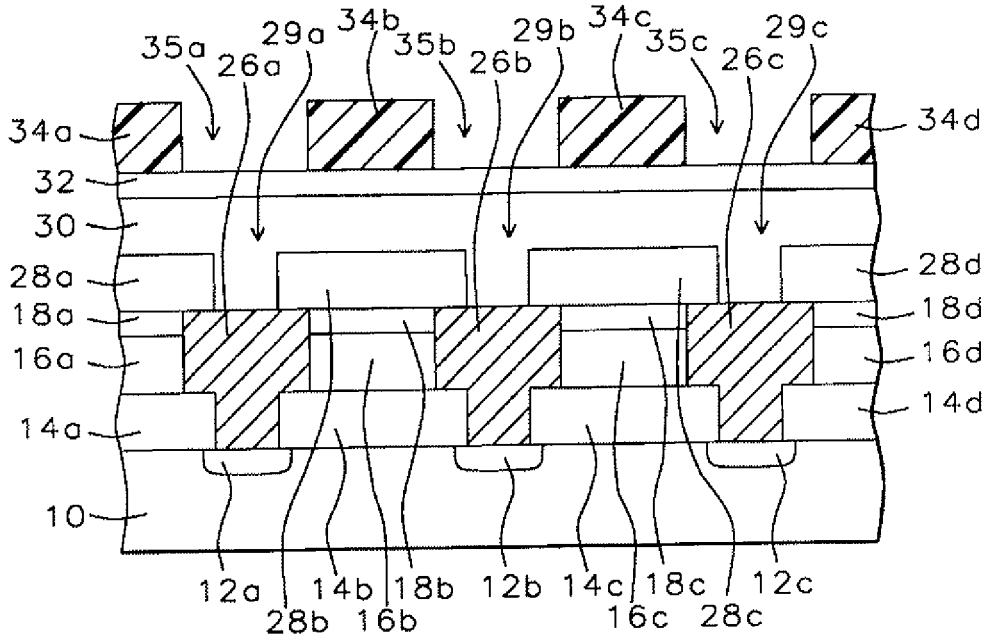
16b 25b 16c 25c

FIG. 3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18a
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16d
14d
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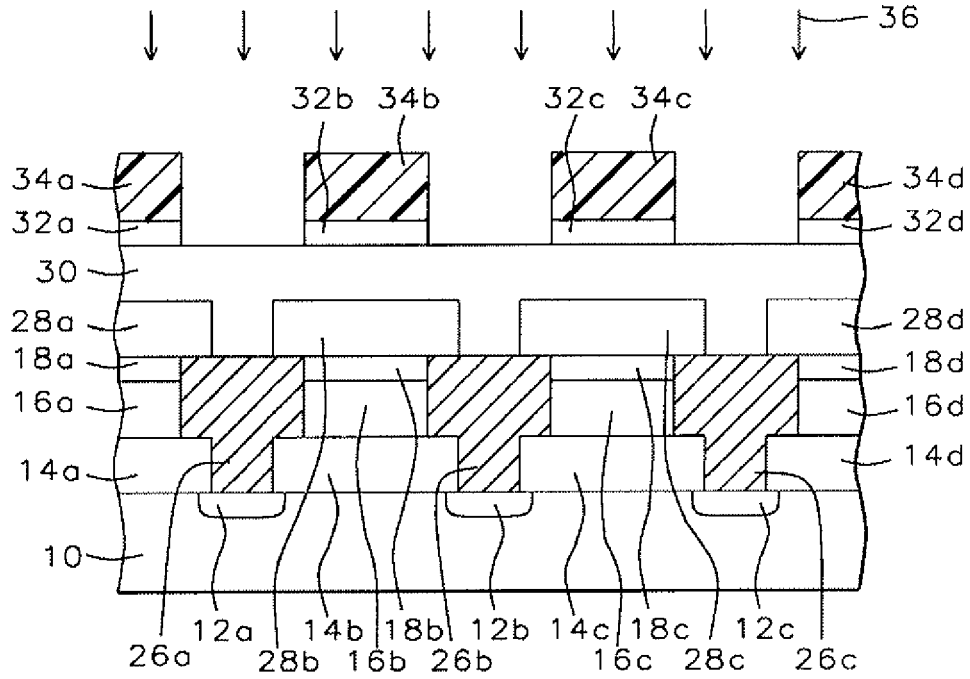
FIG. 4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34a
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18a
16a
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14d
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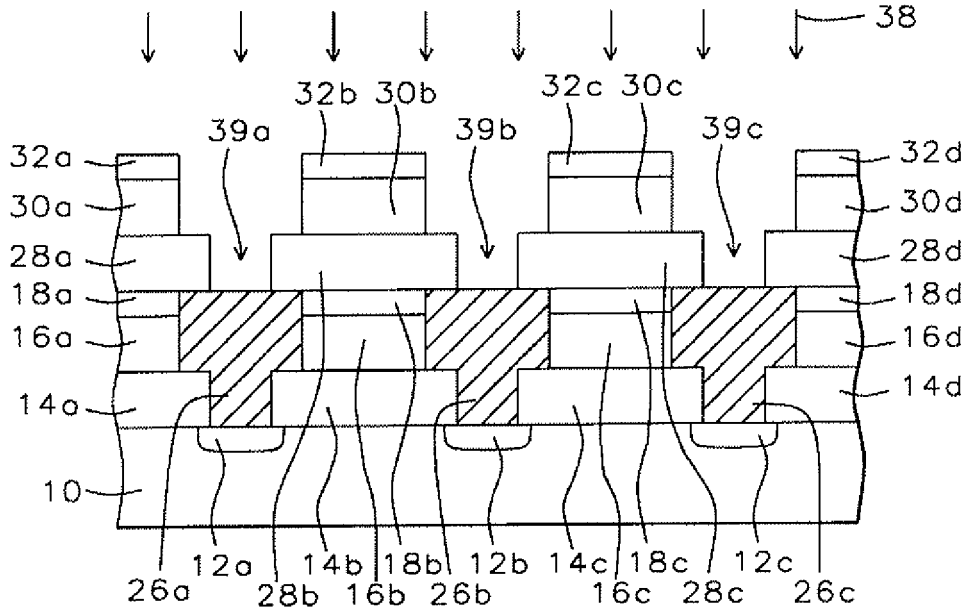
FIG. 5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18d
16d
14d
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16c
18c
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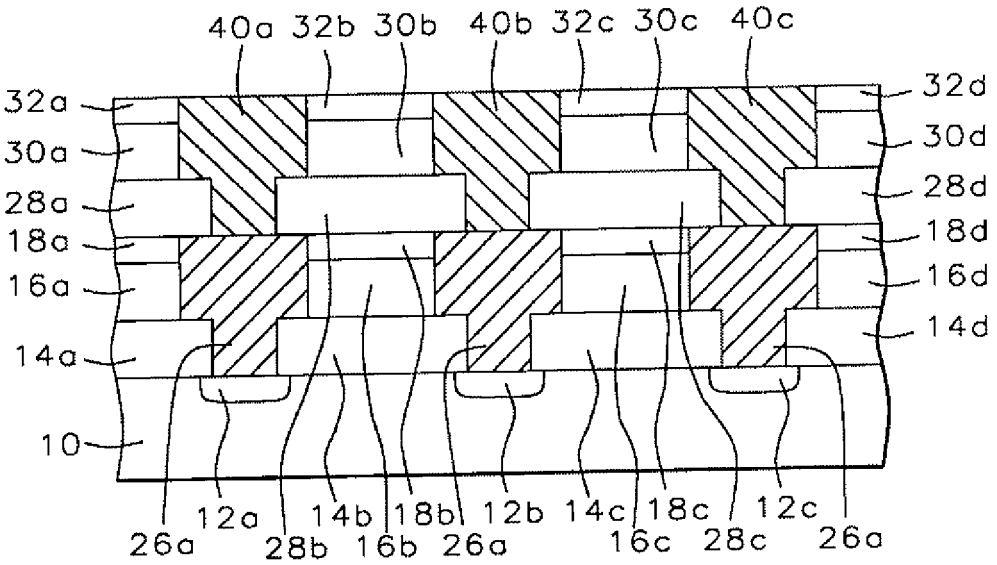
12c
26c

FIG. 6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14a
10
32d
30d
28d
18d
16d
14d
26a 12a 28b 14b 16b 18b 26a 12b 14c 16c 18c 28c 12c 26a

FIG. 7

DUAL DAMASCENE PATTERNED CONDUCTOR LAYER FORMATION METHOD WITHOUT ETCH STOP LAYER

CROSS-REFERENCE TO RELATED APPLICATION

This application is related to a co-assigned and co-invented application Ser. No. 09/177,187 attorney docket number TSMC 97-353, filed Oct. 23, 1998, and similarly titled "Dual Damascene Patterned Conductor Layer Formation Method Without Etch Stop Layer," the teachings of which are incorporated herein by reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates generally to methods for forming patterned conductor layers separated by patterned dielectric layers within microelectronics fabrications. More particularly, the present invention relates to dual damascene methods for forming patterned conductor layers separated by patterned dielectric layers within microelectronics fabrications.

2. Description of the Related Art

Microelectronics fabrications are formed from microelectronics substrates over which are formed patterned microelectronics conductor layers which are separated by microelectronics dielectric layers.

As microelectronics integration levels have increased and microelectronics device and patterned conductor layer dimensions have decreased, it has become increasingly common within the art of microelectronics fabrication to employ, interposed between the patterns of narrow linewidth dimension and/or narrow pitch dimension patterned microelectronics, conductor layers within microelectronics fabrications microelectronics dielectric layers formed of low dielectric constant dielectric materials. Such patterned microelectronics conductor layers often access within the microelectronics fabrications within which they are formed patterned conductor contact stud layers or patterned conductor interconnection stud layers. For the purposes of the present disclosure, low dielectric constant dielectric materials are intended as dielectric materials having a dielectric constant of less than about 3.0. For comparison purposes, dielectric layers formed employing conventional silicon oxide dielectric materials, silicon nitride dielectric materials or silicon oxynitride dielectric materials typically have dielectric constants in the range of from about 4.0 to about 7.0.

Microelectronics dielectric layers formed of low dielectric constant dielectric materials are desirable interposed between the patterns of narrow linewidth dimension and/or narrow pitch dimension patterned microelectronics conductor layers within microelectronics fabrications since such dielectric layers formed from such low dielectric constant dielectric materials provide dielectric layers which assist in providing microelectronics fabrications exhibiting enhanced microelectronics fabrication speed, attenuated patterned microelectronics conductor layer parasitic capacitance, and attenuated patterned microelectronics conductor layer cross-talk.

Low dielectric constant dielectric materials which may be employed for forming low dielectric constant microelectronics dielectric layers within microelectronics fabrications are typically materials with hydrogen and/or carbon content, such as but not limited to organic polymer spin-on-polymer dielectric materials (such as but not limited to polyimide organic polymer spin-on-polymer dielectric materials, poly-arylene-ether organic polymer spin-on-polymer dielectric materials, and fluorinated poly-arylene-ether organic polymer spin-on-polymer dielectric materials), amorphous carbon dielectric materials (such as but not limited to amorphous carbon and fluorinated amorphous carbon), and silsesquioxane spin-on-glass (SOG) dielectric materials (such as but not limited to hydrogen silsesquioxane spin-on-glass (SOG) dielectric materials, carbon bonded hydrocarbon silsesquioxane spin-on-glass (SOG) dielectric materials, and carbon bonded fluorocarbon silsesquioxane spin-on-glass (SOG) dielectric materials).

While organic polymer spin-on-polymer dielectric materials, amorphous carbon dielectric materials, and silsesquioxane spin-on-glass (SOG) dielectric materials are thus desirable within the art of microelectronics fabrication for forming patterned low dielectric constant microelectronics dielectric layers interposed between the patterns of patterned conductor layers which access patterned conductor stud layers within microelectronics fabrications, such microelectronics fabrication structures are often not formed entirely without problems. In particular, such microelectronics fabrication structures are typically formed employing an etch stop layer formed interposed between: (1) a patterned first dielectric layer through which is formed a patterned conductor stud layer; and (2) a patterned low dielectric constant dielectric layer which is formed adjoining the patterned conductor layer which contacts the patterned conductor stud layer. The etch stop layer typically assures optimal definition of the patterned conductor layer within respect to the patterned conductor stud layer. Unfortunately, the presence of such etch stop layers often provides additional microelectronics fabrication complexity within microelectronics fabrications within which are formed patterned conductor layers which contact patterned conductor stud layers.

It is thus towards the goal of forming microelectronics fabrication structures comprising patterned low dielectric constant dielectric layers separating patterned conductor layers which in turn contact patterned conductor stud layers, with attenuated microelectronics fabrication complexity, that the present invention is directed.

Various methods have been disclosed in the art of microelectronics fabrication for forming patterned microelectronics layers within microelectronics fabrications.

For example, Korczynski, in "Low-k dielectric integration cost modelling," Solid State Technology, Oct. 1997, pp. 123–28, discloses in general various methods and materials for forming patterned low dielectric constant dielectric layers interposed between the patterns of patterned conductor layers which in turn contact patterned conductor stud layers within microelectronics fabrications. Disclosed are standard patterned conductor layer formation and dielectric layer isolation methods and dual damascene patterned conductor layer formation and dielectric layer isolation methods.

In addition, Krishnan et al., in U.S. Pat. No. 5,380,546, discloses a maskless method for forming a barrier layer surrounded metal feature within a planar insulator layer within a microelectronics fabrication. The barrier layer surrounded metal feature so formed is formed employing a planarizing method rather than a masking method.

Further, Ireland, in U.S. Pat. No. 5,466,639, discloses a dual damascene method for forming a patterned conductor layer contiguous with a patterned conductor stud layer within a semiconductor integrated circuit microelectronics fabrication. The dual damascene method employs a pat-

terned mask layer formed interposed between a lower dielectric layer through which is formed the patterned conductor stud layer and an upper dielectric layer through which is formed the patterned conductor layer contiguous with the patterned conductor stud layer, where the upper dielectric layer and the lower dielectric layer are patterned employing a single reactive ion etch method.

Yet further, Havemann, in U.S. Pat. No. 5,565,384, discloses a method for forming within an integrated circuit microelectronics fabrication a self-aligned via through an inorganic dielectric layer to access a patterned conductor layer formed below the inorganic dielectric layer, where the patterned conductor layer has interposed at least partially between its patterns an organic containing dielectric layer. The patterned conductor layer and the organic dielectric layer are completely covered by the inorganic dielectric layer. The method employs an anisotropic etchant which is selective to the inorganic dielectric layer with respect to the organic dielectric layer, such that the organic dielectric layer serves as an etch stop layer when etching the self-aligned via through the inorganic dielectric layer, thus avoiding overetching of the organic dielectric layer.

Still yet further, Huang et al., in U.S. Pat. No. 5,635,423 also discloses a dual damascene method for forming a patterned conductor layer contiguous with a patterned conductor stud layer within a semiconductor integrated circuit microelectronics fabrication. The dual damascene method employs a blanket mask layer formed interposed between a lower dielectric layer through which is formed the patterned conductor stud layer and an upper dielectric layer through which is formed the patterned conductor layer contiguous with the patterned conductor stud layer, where the upper dielectric layer and the lower dielectric layer are sequentially patterned employing separate reactive ion etch (RIE) methods.

Finally, Avanzino et al., in U.S. Pat. No. 5,686,354, discloses yet another dual damascene method for forming a patterned conductor layer contiguous with a patterned conductor stud layer within a microelectronics fabrication. The dual damascene method employs a single dielectric layer sequentially: (1) partially patterned employing a first etch method to form a trench within the single dielectric layer; and (2) subsequently completely patterned employing a second etch method and hard mask layer exposing a portion of a floor within the trench, to define with sharp sidewall edges the patterned conductor stud layer through the single dielectric layer.

Desirable in the art of microelectronics fabrication are methods through which there may be formed within microelectronics fabrications low dielectric constant dielectric layers interposed between the patterns of patterned conductor layers which in turn contact patterned conductor stud layers, with attenuated process complexity.

It is towards the foregoing object that the present invention is both generally and more specifically directed.

SUMMARY OF THE INVENTION

A first object of the present invention is to provide a method for forming within a microelectronics fabrication a patterned low dielectric constant dielectric layer adjoining a patterned conductor layer which in turn contacts a patterned conductor stud layer.

A second object of the present invention is to provide a method in accord with the first object of the present invention, where the method provides for attenuated process complexity.

A third object of the present invention is to provide a method in accord with the first object of the present invention or the second object of the present invention, where the microelectronics fabrication is a semiconductor integrated circuit microelectronics fabrication.

A fourth object of the present invention is to provide a method in accord with the first object of the present invention, the second object of the present invention or the third object of the present invention, which method is readily commercially implemented.

In accord with the objects of the present invention, there is provided by the present invention a method for forming a via through a dielectric layer within a microelectronics fabrication. To practice the method of the present invention, there is first provided a substrate employed within a microelectronics fabrication, where the substrate has a contact region formed therein. There is then formed upon the substrate a patterned first dielectric layer, where the patterned first dielectric layer defines a via accessing the contact region. The patterned first dielectric layer is formed from a first dielectric material which is not susceptible to etching within an oxygen containing plasma. There is then formed upon the patterned first dielectric layer a blanket second dielectric layer, where the blanket second dielectric layer completely covers the patterned first dielectric layer and fills the via. The blanket second dielectric layer is formed from a second dielectric material which is susceptible to etching within the oxygen containing plasma. There is then formed upon the blanket second dielectric layer a blanket hard mask layer, where the blanket hard mask layer is formed from a hard mask material which is not susceptible to etching within the oxygen containing plasma. There is then formed upon the blanket hard mask layer a patterned photoresist layer, where the patterned photoresist layer leaves exposed a portion of the blanket hard mask layer greater that an areal dimension of the via and at least partially overlapping the areal dimension of the via. There is then etched while employing a first plasma etch method the blanket hard mask layer to form a patterned hard mask layer defining a first trench formed through the patterned hard mask layer while employing the patterned photoresist layer as a first etch mask layer. The first plasma etch method employs a first etchant gas composition appropriate to the hard mask material from which is formed the blanket hard mask layer. Finally, there is then etched while employing a second plasma etch method the blanket second dielectric layer to form a patterned second dielectric layer defining an aperture formed therethrough. The aperture comprises: (1) a second trench corresponding with the first trench; and (2) at least a portion of the first via. The second plasma etch method employs the oxygen containing plasma. There may subsequently be formed within the aperture a patterned conductor layer within the second trench contiguous with a conductor stud layer within the via while employing a damascene method.

The present invention provides a method for forming within a microelectronics fabrication a patterned low dielectric constant dielectric layer adjoining a patterned conductor layer which in turn contacts a patterned conductor stud layer, where the method provides for attenuated process complexity. The method of the present invention realizes the foregoing objects by employing when forming the patterned low dielectric constant dielectric layer a low dielectric constant dielectric material which is etchable within an oxygen containing plasma. The patterned low dielectric constant dielectric layer so formed is formed upon a patterned first dielectric layer which is not etchable within the oxygen

containing plasma, where the patterned first dielectric layer defines a via accessing a contact region within a substrate layer formed beneath the patterned first dielectric layer. Thus, when employing an appropriate hard mask layer and an oxygen containing plasma etch method employing the oxygen containing plasma, there may be formed without employing an etch stop layer interposed between the patterned first dielectric layer and the low dielectric constant dielectric layer an aperture through the low dielectric constant dielectric layer and the patterned first dielectric layer, which aperture comprises: (1) a trench within the low dielectric constant dielectric layer; and (2) at least a portion of the via. The aperture so formed may subsequently have formed therein a patterned conductor layer contiguous with a patterned conductor stud layer while employing a damascene method. Thus, the present invention provides a method for forming within a microelectronics fabrication a patterned low dielectric constant dielectric layer adjoining a patterned conductor layer which in turn contacts and is contiguous with a patterned conductor stud layer, where the method provides for attenuated process complexity.

The present invention may be employed where the microelectronics fabrication is a semiconductor integrated circuit microelectronics fabrication. The present invention does not discriminate with respect to the nature of a microelectronics fabrication within which is formed a patterned low dielectric constant dielectric layer interposed between the patterns of a patterned conductor layer which in turn contacts a patterned conductor stud layer. Thus, although the method of the present invention may be employed when forming patterned low dielectric constant dielectric layers interposed between the patterns of patterned conductor layers which in turn contact patterned conductor stud layers within semiconductor integrated circuit microelectronics fabrications, the method of the present invention may also be employed in forming patterned low dielectric constant dielectric layers interposed between the patterns of patterned conductor layers which in turn contact patterned conductor stud layers within microelectronics fabrications including but not limited to semiconductor integrated circuit microelectronics fabrications, solar cell microelectronics fabrications, ceramic substrate microelectronics fabrications and flat panel display microelectronics fabrications.

The present invention is readily commercially implemented. The method of the present invention employs methods and materials which are otherwise generally known in the art of microelectronics fabrication. Since it is a novel ordering and use of methods and materials which provides the method of the present invention, rather than the existence of the methods and materials which provides the present invention, the method of the present invention is readily commercially implemented.

BRIEF DESCRIPTION OF THE DRAWINGS

The objects, features and advantages of the present invention are understood within the context of the Description of the Preferred Embodiment, as set forth below. The Description of the Preferred Embodiment is understood within the context of the accompanying drawings, which form a material part of this disclosure, wherein:

FIG. 1 to FIG. 7 show a series of schematic cross-sectional diagrams illustrating the results of forming within a microelectronics fabrication in accord with a preferred embodiment of the present invention two series of patterned low dielectric constant dielectric layers interposed between two series of patterned conductor layers in turn contacting two series of patterned conductor stud layers, in accord with the method of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention provides a method for forming within a microelectronics fabrication a patterned low dielectric constant dielectric layer adjoining a patterned conductor layer which in turn contacts a patterned conductor stud layer, where the method provides for attenuated process complexity. The method of the present invention realizes the foregoing objects by employing when forming the patterned low dielectric constant dielectric layer a low dielectric constant dielectric material which is etchable within an oxygen containing plasma. The patterned low dielectric constant dielectric layer so formed is formed upon a patterned first dielectric layer which is not etchable within the oxygen containing plasma, where the patterned first dielectric layer defines a via accessing a contact region within a substrate layer formed beneath the patterned first dielectric layer. Thus, when employing an appropriate hard mask layer and an oxygen containing plasma etch method employing the oxygen containing plasma, there may be formed without employing an etch stop layer interposed between the patterned first dielectric layer and the low dielectric constant dielectric layer an aperture through the low dielectric constant dielectric layer and the patterned first dielectric layer, where the aperture comprises: (1) a trench within the low dielectric constant dielectric layer; and (2) at least a portion of the via. The aperture so formed may subsequently have formed therein a patterned conductor layer contiguous with a patterned conductor stud layer while employing a damascene method.

The present invention does not discriminate with respect to the nature of a microelectronics fabrication within which is formed a patterned low dielectric constant dielectric layer interposed between the patterns of a patterned conductor layer which in turn contacts a patterned conductor stud layer. Thus, although the method of the present invention may be employed when forming patterned low dielectric constant dielectric layers interposed between the patterns of patterned conductor layers which in turn contact patterned conductor stud layers within semiconductor integrated circuit microelectronics fabrications, the method of the present invention may also be employed in forming patterned low dielectric constant dielectric layers interposed between the patterns of patterned conductor layers which in turn contact patterned conductor stud layers within microelectronics fabrications including but not limited to semiconductor integrated circuit microelectronics fabrications, solar cell microelectronics fabrications, ceramic substrate microelectronics fabrications and flat panel display microelectronics fabrications.

Referring now to FIG. 1 to FIG. 7, there is shown a series of schematic cross-sectional diagrams illustrating the results of forming within a microelectronics fabrication in accord with a preferred embodiment of the present invention two series of patterned low dielectric constant dielectric layers interposed between two series of patterned conductor layers which in turn contact two series of patterned conductor stud layers, formed in accord with the method of the present invention. Shown in FIG. 1 is a schematic cross-sectional diagram of the microelectronics fabrication at an early stage in its fabrication in accord with the method of the present invention.

Shown in FIG. 1 is a substrate 10 employed within a microelectronics fabrication, where the substrate 10 has

formed therein a series of contact regions **12***a*, **12***b*, and **12***c*. Within the preferred embodiment of the present invention, the substrate **10** may be a substrate employed within a microelectronics fabrication including but not limited to a semiconductor integrated circuit microelectronics fabrication, a solar cell microelectronics fabrication, a ceramic substrate microelectronics fabrication or a flat panel display microelectronics fabrication. Although not specifically illustrated within the schematic cross-sectional diagram of FIG. **1**, the substrate **10** may be the substrate itself employed within the microelectronics fabrication, or in the alternative, the substrate **10** may be the substrate employed within the microelectronics fabrication, where the substrate has any of several additional layers formed thereupon or thereover as are conventional within the microelectronics fabrication within which is employed the substrate. Such additional microelectronics layers may include, but are not limited to, microelectronics conductor layers, microelectronics semiconductor layers and microelectronics dielectric layers.

With respect to the contact regions **12***a*, **12***b*, and **12***c* formed within the substrate **10**, the contact regions **12***a*, **12***b*, and **12***c* will typically be either conductor contact regions or semiconductor contact regions within the microelectronics fabrication within which is employed the substrate **10**. More preferably, within the present invention when the substrate **10** is a semiconductor substrate alone employed within a semiconductor integrated circuit microelectronics fabrication, and the contact regions **12***a*, **12***b*, and **12***c* are semiconductor substrate contact regions which are typically employed when forming semiconductor integrated circuit devices employing the substrate **10**.

Shown also within FIG. **1** formed upon the substrate **10** is a series of patterned first dielectric layers **14***a*, **14***b*, **14***c*, and **14***d* which define a series of first vias **15***a*, **15***b*, and **15***c* which in turn access the series of contact regions **12***a*, **12***b*, and **12***c*. Within the first preferred embodiment of the present invention, the series of patterned first dielectric layers **14***a*, **14***b*, **14***c*, and **14***d* is formed of a first dielectric material which is not susceptible to etching within an oxygen containing plasma. Many dielectric materials which possess this property are known in the art of microelectronics fabrication, such dielectric materials including but not limited to silicon oxide dielectric materials, silicon nitride dielectric materials, and silicon oxynitride dielectric materials which may be formed employing methods including but not limited to chemical vapor deposition (CVD) methods, plasma enhanced chemical vapor deposition (PECVD) methods and physical vapor deposition (PVD) sputtering methods. Thus, although other methods and materials may be employed, the patterned first dielectric layers **14***a*, **14***b*, **14***c*, and **14***d* are preferably formed of a silicon oxide dielectric material deposited employing a chemical vapor deposition (CVD) method, as is conventional in the art of microelectronics fabrication. Preferably, each of the patterned first dielectric layers **14***a*, **14***b*, **14***c*, and **14***d* so formed is formed to a thickness of from about 5000 to about 9000 angstroms. Preferably, each of the first vias **15***a*, **15***b*, or **15***c* has a linewidth of from about 0.2 to about 0.5 microns.

Also shown in FIG. **1** formed upon the patterned first dielectric layers **14***a*, **14***b*, **14***c*, and **14***d*, and portions of the contact regions **12***a*, **12***b*, and **12***c* exposed within the corresponding series of first vias **15***a*, **15***b* and **15***c* is a blanket second dielectric layer **16**. Within the preferred embodiment of the present invention, the blanket second dielectric layer **16** is formed of a second dielectric material which is susceptible to etching within the oxygen containing plasma within which the patterned first dielectric layers **14***a*, **14***b*, **14***c*, and **14***d* are not susceptible to etching. For the purposes of defining an extent to which the patterned first dielectric layers **14***a*, **14***b*, **14***c*, and **14***d* are not susceptible to etching within the oxygen containing plasma while the blanket second dielectric layer **16** is susceptible to etching within the oxygen containing plasma, the blanket first dielectric layer **16** preferably has an etch rate ratio within the oxygen containing plasma with respect to the patterned first dielectric layers **14***a*, **14***b*, **14***c*, and **14***d* of greater than about 20:1, more preferably greater than about 30:1, and most preferably greater than about 50:1. Although not specifically illustrated within the schematic cross-sectional diagram of FIG. **1**, the blanket second dielectric layer **16** may optionally, if desirable, be planarized employing an appropriate planarizing method.

Within the preferred embodiment of the present invention, the blanket second dielectric layer **16**, which is formed of the second dielectric material which is susceptible to etching within the oxygen containing plasma is preferably formed of a low dielectric constant dielectric material selected from the group including but not limited to organic polymer spin-on-polymer dielectric materials (such as but not limited to polyimide organic polymer spin-on-polymer dielectric materials, poly-arylene-ether organic polymer spin-on-polymer dielectric materials and fluorinated poly-arylene-ether organic polymer spin-on-polymer dielectric materials) and amorphous carbon dielectric materials (such as but not limited to amorphous carbon and fluorinated amorphous carbon). Preferably, the blanket second dielectric layer **16** is formed to a thickness of from about 4000 to about 7000 angstroms.

There is also shown in FIG. **1** a blanket first hard mask layer **18** formed upon the blanket second dielectric layer **16**. Within the preferred embodiment of the present invention, the blanket first hard mask layer **18** is formed of a hard mask material which is also not susceptible to etching within the oxygen containing plasma. Similarly with the patterned first dielectric layers **14***a*, **14***b*, **14***c*, and **14***d*, there are several methods and materials which may be employed in forming the blanket first hard mask layer **18**, where such methods and materials include but are not limited to thermally assisted evaporation methods, electron beam assisted evaporation methods, chemical vapor deposition (CVD) methods and physical vapor deposition (PVD) sputtering methods which may be employed for forming blanket hard mask layers from hard mask materials including but not limited to conductor hard mask materials, semiconductor hard mask materials, and insulator hard mask materials. Although the blanket first hard mask layer **18** may be formed employing any of several such methods and materials as are known in the art of microelectronics fabrication, the blanket first hard mask layer **18** is typically and preferably formed of a hard mask material analogous or equivalent to the dielectric material from which is formed the patterned first dielectric layers **14***a*, **14***b*, **14***c*, and **14***d*. Preferably, the blanket first hard mask layer **18** so formed is formed to a thickness of from about 500 to about 2000 angstroms.

Finally, there is also shown in FIG. **1** the presence of a series of patterned first photoresist layers **20***a*, **20***b*, **20***c*, and **20***d* formed upon the blanket first hard mask layer **18**. Within the first preferred embodiment of the present invention, the patterned first photoresist layers **20***a*, **20***b*, **20***c*, and **20***d* may be formed from any of several photoresist materials as are generally known in the art of microelectronics fabrication, including photoresist materials selected from the general

groups of photoresist materials including but not limited to positive photoresist materials and negative photoresist materials. For the preferred embodiment of the present invention, the patterned first photoresist layers **20***a*, **20***b*, **20***c*, and **20***d* are preferably formed of a positive photoresist material as is conventional in the art of microelectronics fabrication, in order to assure optimal dimensional stability. Preferably, the patterned first photoresist layers **20***a*, **20***b*, **20***c*, and **20***d* so formed are formed to a thickness of from about 7000 to about 15000 angstroms.

Although not completely illustrated within the schematic cross-sectional diagram of FIG. **1**, the patterned first photoresist layers **20***a*, **20***b*, **20***c* and **20***d* define a series of first trenches **21***a*, **21***b*, and **21***c* leaving exposed a portion of the blanket first hard mask layer **18** of areal dimension greater than the areal dimension of a corresponding first via **15***a*, **15***b*, or **15***c*, while simultaneously at least partially overlapping the areal dimension of the corresponding first vias **15***a*, **15***b*, or **15***c*. More preferably, as illustrated within the schematic cross-sectional diagram of FIG. **1**, the areal dimension of each first trench **21***a*, **21***b*, or **21***c* within the series of first trenches **21***a*, **21***b*, and **21***b* completely overlaps and encompasses the areal dimension of a corresponding first via **15***a*, **15***b*, or **15***c* within the series of first vias **15***a*, **15***b* and **15***c*.

Referring now to FIG. **2**, there is shown a schematic cross-sectional diagram illustrating the results of further processing of the microelectronics fabrication whose schematic cross-sectional diagram is illustrated in FIG. **1**. Shown in FIG. **2** is a schematic cross-sectional diagram of a microelectronics fabrication otherwise equivalent to the microelectronics fabrication whose schematic cross-sectional diagram is illustrated in FIG. **1**, but wherein the blanket first hard mask layer **18** has been patterned to form a series of patterned first hard mask layers **18***a*, **18***b*, **18***c*, and **18***d*, through etching while employing a first plasma **22** in conjunction with the patterned first photoresist layers **20***a*, **20***b*, **20***c*, and **20***d* as a first photoresist etch mask layer. Within the preferred embodiment of the present invention, the first plasma **22** preferably employs an etchant gas composition appropriate to the material from which is formed the blanket first hard mask layer **18**. When the blanket first hard mask layer **18** is formed from a silicon oxide dielectric material, as is preferred within the preferred embodiment of the present invention, the first plasma **22** preferably employs a fluorine containing (such as but not limited to fluorocarbon containing) etchant gas composition. Under such circumstances, the first plasma **22** more preferably employs a carbon tetrafluoride, hexafluoroethane and argon containing etchant gas composition.

Preferably, the first plasma **22** is employed within a first plasma etch method which also employs: (1) a reactor chamber pressure of from about 2 to about 8 mtorr; (2) a source radio frequency power of from about 1000 to about 2000 watts at a radio frequency of 13.56 MHZ; (3) a bias power of from about 1000 to about 2000 watts; (4) a carbon tetrafluoride flow rate of from about 10 to about 20 standard cubic centimeters per minute (sccm); (5) a hexafluoroethane flow rate of from about 10 to about 20 standard cubic centimeters per minute (sccm); and (6) an argon flow rate of from about 100 to about 300 standard cubic centimeters per minute (sccm), for a time sufficient to form from the blanket first hard mask layer **18** the corresponding series of patterned first hard mask layers **18***a*, **18***b*, **18***c* and **18***d*.

Referring now to FIG. **3**, there is shown a schematic cross-sectional diagram illustrating the results of further processing of the microelectronics fabrication whose schematic cross-sectional diagram is illustrated in FIG. **2**. Shown in FIG. **3** is a schematic cross-sectional diagram of a microelectronics fabrication otherwise equivalent to the microelectronics fabrication whose schematic cross-sectional diagram is illustrated in FIG. **2**, but wherein: (1) the patterned first photoresist layers **20***a*, **20***b*, **20***c*, and **20***d* are stripped from the microelectronics fabrication; and (2) the blanket second dielectric layer **16** is patterned to form the patterned second dielectric layers **16***a*, **16***b*, **16***c*, and **16***d*, while simultaneously forming a series of first apertures **25***a*, **25***b*, and **25***c* which access the corresponding contact regions **12***a*, **12***b* and **12***c*, while employing a second plasma **24** and at least the patterned hard mask layers **18***a*, **18***b*, **18***c*, and **18***d* as a second etch mask layer.

Within the preferred embodiment of the present invention, the second plasma **24** is the oxygen containing plasma within which neither the series of patterned first dielectric layers **14***a*, **14***b*, **14***c*, and **14***d* nor the blanket first hard mask layer **18** is susceptible to etching, but wherein the blanket second dielectric layer **16** is susceptible to etching.

Within the preferred embodiment of the present invention, the second plasma **24** preferably employs an oxygen containing etchant gas composition comprising an oxygen containing etchant gas selected from the group including but not limited to oxygen, ozone, nitrous oxide and nitric oxide. More preferably, the second plasma **24** employs an oxygen containing etchant gas comprising oxygen along with argon, where argon is employed at a sputter gas component. Preferably, the second plasma **24** is employed within a second plasma etch method which also employs: (1) a reactor chamber pressure of from about 2 to about 10 mtorr; (2) a radio frequency source power of from about 500 to about 1500 watts at a radio frequency of 13.56 MHZ; (3) a bias power of from about 1000 to about 2000 watts; (4) an oxygen flow rate of from about 10 to about 50 standard cubic centimeters per minute (sccm); (5) an argon flow rate of from about 5 to about 20 standard cubic centimeters per minute (sccm); and (6) an optional helium and/or hexafluoroethane flow rate of from about 1 to about 5 standard cubic centimeters per minute (sccm) each.

Although as illustrated within the schematic cross-sectional diagram of FIG. **3** the patterned first photoresist layers **20***a*, **20***b*, **20***c*, and **20***d* are stripped from the microelectronics fabrication whose schematic cross sectional diagram is illustrated in FIG. **2** simultaneously with patterning the blanket second dielectric layer **16** to form the patterned second dielectric layers **16***a*, **16***b*, **16***c* and **16***d*, it is also feasible within the present invention that the patterned first photoresist layers **20***a*, **20***b*, **20***c*, and **20***d* may be stripped from the patterned first hard mask layers **18***a*, **18***b*, **18***c*, and **18***d* prior to patterning the blanket second dielectric layer **16** to form the patterned second dielectric layers **16***a*, **16***b*, **16***c*, and **16***d* while employing the second plasma **24**. Under such circumstances there is typically employed for stripping the patterned first photoresist layers **20***a*, **20***b*, **20***c*, and **20***d* a wet chemical photoresist stripper which does not etch the blanket second dielectric layer **16**. Although such an independent stripping of the patterned first photoresist layers **20***a*, **20***b*, **20***c*, and **20***d* adds process complexity to the method of the present invention, the use of the patterned first hard mask layers **18***a*, **18***b*, **18***c*, and **18***d* alone as an etch mask layer in conjunction with the second plasma **24** will typically provide better definition of the series of first apertures **25***a*, **25***b*, and **25***c* which comprise: (1) a series of trenches corresponding with the series of first trenches **21***a*, **21***b*, and **21***c* defined by the series of patterned first photoresist layers **20***a*, **20***b*, **20***c*, and **20***d*; and (2) the series of first vias **15***a*, **15***b*, and **15***c*.

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Under circumstances where the patterned first photoresist layers **20***a*, **20***b*, **20***c*, and **20***d* are stripped from the microelectronics fabrication whose schematic cross-sectional diagram is illustrated in FIG. **2** simultaneously with etching the blanket second dielectric layer **16** to form the patterned second dielectric layers **16***a*, **16***b*, **16***c*, and **16***d*, there is preferably employed within the preferred embodiment of the present invention a thickness of the patterned photoresist layers **20***a*, **20***b*, **20***c*, and **20***d* such that the patterned first photoresist layers **20***a*, **20***b*, **20***c*, and **20***d* are completely stripped from the corresponding patterned first hard mask layers **18***a*, **18***b*, **18***c*, and **18***d* without need for overetching the series of patterned second dielectric layers **16***a*, **16***b*, **16***c*, and **16***d*. Under such circumstances, optimal lateral dimensional integrity of the series of patterned second dielectric layers **16***a*, **16***b*, **16***c*, and **16***d* is facilitated. Similarly, the use of the argon sputtering gas component within the second plasma **24** also assists in facilitating optimal lateral dimensional integrity of the patterned second dielectric layers **16***a*, **16***b*, **16***c*, and **16***d*.

Referring now to FIG. **4**, there is shown a schematic cross-sectional diagram illustrating the results of further processing of the microelectronics fabrication whose schematic cross-sectional diagram is illustrated in FIG. **3**. Shown in FIG. **4** is a schematic cross-sectional diagram of a microelectronics fabrication otherwise equivalent to the microelectronics fabrication whose schematic cross-sectional diagram is illustrated in FIG. **3**, but wherein there is formed into the series of first apertures **25***a*, **25***b*, and **25***c* a series of patterned conductive contact stud layers **26***a*, **26***b*, and **26***c* contacting the respective contact regions **12***a*, **12***b*, and **12***c* within the substrate **10**. Within the preferred embodiment of the present invention, the series of patterned conductive contact stud layers **26***a*, **26***b*, and **26***c* is formed into the series of apertures **25***a*, **25***b*, and **25***c* employing a damascene method. Within the damascene method, a blanket conductive contact stud layer is formed upon the patterned hard mask layers **18***a*, **18***b*, **18***c*, and **18***d* and into the apertures **25***a*, **25***b*, and **25***c*, and subsequently planarized, typically employing an appropriate polishing method. For the preferred embodiment of the present invention, the patterned conductive contact stud layers **26***a*, **26***b*, and **26***c* may be formed of any conductive material which is conventionally employed for forming conductive contact stud layers within the microelectronics fabrication within which is employed the substrate **10**. Such conductive materials may include, but are not limited to metals, metal alloys, metal composites, metal alloy composites, doped polysilicon and polycides (doped polysilicon/metal silicide stacks), beneath and/or above which may optionally be formed barrier layers, as are conventional in the art of microelectronics fabrication.

Shown also in FIG. **4** formed upon the patterned hard mask layers **18***a*, **18***b*, **18***c*, and **18***d*, and the patterned conductive stud layers **26***a*, **26***b*, and **26***c*, is a series of patterned third dielectric layers **28***a*, **28***b*, **28***c*, and **28***d* which define a series of second vias **29***a*, **29***b*, and **29***c* which access portions of the corresponding patterned conductive contact stud layers **26***a*, **26***b*, and **26***c*. Similarly, there is also shown in FIG. **4** formed upon the patterned third dielectric layers **28***a*, **28***b*, **28***c*, and **28***d*, and portions of the patterned conductive contact stud layers **26***a*, **26***b*, and **26***c* exposed within the corresponding vias **29***a*, **29***b*, and **29***c* a blanket fourth dielectric layer **30**. In addition, there is shown in FIG. **4** formed upon the blanket fourth dielectric layer **30** a blanket second hard mask layer **32**. Finally, there is shown in FIG. **4** formed upon the blanket second hard mask layer **32** a series of patterned second photoresist layers **34***a*, **34***b*, **34***c*, and **34***d*.

Within the preferred embodiment of the present invention, the series of patterned third dielectric layers **28***a*, **28***b*, **28***c*, and **28***d* is preferably formed employing methods, materials and dimensions analogous or equivalent to the methods, materials and dimensions employed in forming the series of patterned first dielectric layers **14***a*, **14***b*, **14***c*, and **14***d* as illustrated within the schematic cross-sectional diagram of FIG. **1**. Similarly, within the preferred embodiment of the present invention the blanket fourth dielectric layer **30** is preferably formed employing methods, materials and dimensions analogous or equivalent to the methods, materials, and dimensions employed in forming the blanket second dielectric layer **16** as illustrated within the schematic cross sectional diagram of FIG. **1**. In addition, within the second preferred embodiment of the present invention, the blanket second hard mask layer **32** is preferably formed employing methods, materials and dimensions analogous or equivalent to the methods, materials, materials, and dimensions employed in forming the blanket first hard mask layer **18** as illustrated within the schematic cross-sectional diagram of FIG. **1**. Finally, within the second preferred embodiment of the present invention, the series of second photoresist layers **34***a*, **34***b*, **34***c*, and **34***d* is preferably formed employing methods, materials and dimensions analogous or equivalent to the methods, materials and dimensions employed in forming the series of patterned first photoresist layers **20***a*, **20***b*, **20***c*, and **20***d* as illustrated within the schematic cross-sectional diagram of FIG. **1**.

Referring now to FIG. **5**, there is shown a schematic cross-sectional diagram illustrating the results of further processing of the microelectronics fabrication whose schematic cross-sectional diagram is illustrated in FIG. **4**. Shown in FIG. **5** is a schematic cross-sectional diagram of a microelectronics fabrication otherwise equivalent to the microelectronics fabrication whose schematic cross-sectional diagram is illustrated in FIG. **4**, but wherein the blanket second hard mask layer **32** has been patterned to form a series of patterned second hard mask layers **32***a*, **32***b*, **32***c* and **32***d* through etching with a third plasma **36** while employing the series of patterned second photoresist layers **34***a*, **34***b*, **34***c*, and **34***d* as a third etch mask layer, and while employing the blanket fourth dielectric layer **30** as an etch stop layer. Within the preferred embodiment of the present invention, the third plasma **36** is preferably formed employing methods and materials analogous or equivalent to the methods and materials employed in forming the first plasma **22** as illustrated within FIG. **2**. Thus, the series of patterned second hard mask layers **32***a*, **32***b*, **32***c*, and **32***d* as illustrated in FIG. **5** is formed analogously with the series of patterned first hard mask layers **18***a*, **18***b*, **18***c*, and **18***d* as illustrated within the schematic cross-sectional diagram of FIG. **2**.

Referring now to FIG. **6**, there is shown a schematic cross-sectional diagram illustrating the results of further processing of the microelectronics fabrication whose schematic cross-sectional diagram is illustrated in FIG. **5**. Shown in FIG. **6** is a schematic cross-sectional diagram of a microelectronics fabrication otherwise equivalent to the microelectronics fabrication whose schematic cross-sectional diagram is illustrated in FIG. **5**, but wherein: (1) the series of patterned second photoresist layers **34***a*, **34***b*, **34***c* and **34***d* has been stripped from the corresponding series of patterned second hard mask layers **32***a*, **32***b*, **32***c*, and **32***d*; and (2) there is formed from the blanket fourth dielectric layer **30** a series of patterned fourth dielectric layers **30***a*, **30***b*, **30***c*, and **30***d* which defines a series of second apertures **39***a*, **39***b* and **39***c* which access the series of patterned

conductor contact stud layers **26***a*, **26***b*, and **26***c*, while employing a fourth plasma **38** and at least the series of patterned second hard mask layers **32***a*, **32***b*, **32***c*, and **32***d* as a fourth etch mask layer. Within the preferred embodiment of the present invention, the fourth plasma **38** is preferably formed employing methods and materials analogous or equivalent to the methods and materials employed in forming the second plasma **24** as illustrated within the schematic cross-sectional diagram of FIG. **3**. Thus, the series of patterned fourth dielectric layers **30***a*, **30***b*, **30***c*, and **30***d* as illustrated within the schematic cross-sectional diagram of FIG. **6** is formed analogously or equivalently with the series of patterned second dielectric layers **16***a*, **16***b*, **16***c*, and **16***d* as illustrated within the schematic cross-sectional diagram of FIG. **3**.

Referring now to FIG. **7**, there is shown a schematic cross-sectional diagram illustrating the results of further processing of the microelectronics fabrication whose schematic cross-sectional diagram is illustrated in FIG. **6**. Shown in FIG. **7** is a microelectronics fabrication otherwise equivalent to the microelectronics fabrication whose schematic cross-sectional diagram is illustrated in FIG. **6**, but wherein there is formed within the series of second apertures **39***a*, **39***b*, and **39***c* a series of patterned conductive interconnection stud layers **40***a*, **40***b*, and **40***c*. Within the preferred embodiment of the present invention, the series of patterned conductive interconnection stud layers **40***a*, **40***b*, and **40***c* as illustrated within the schematic cross-sectional diagram of FIG. **7** is preferably formed employing methods, materials, and dimensions analogous or equivalent to the methods, materials, and dimensions employed in forming the patterned conductive contact stud layers **26***a*, **26***b*, and **26***c* as illustrated within the schematic cross-sectional diagram of FIG. **4**.

Upon forming the microelectronics fabrication whose schematic cross-sectional diagram is illustrated in FIG. **7**, there is formed a microelectronics fabrication having formed therein two series of low dielectric constant dielectric layers interposed between two series of patterned conductor layers which in turn are contiguous with and contacting two series of patterned conductor stud layers, with attenuated process complexity.

As is understood by a person skilled in the art, the preferred embodiment of the present invention is illustrative of the present invention rather than limiting of the present invention. Revisions and modifications may be made to methods, materials, structures, and dimensions through which may be formed microelectronics fabrications in accord with the preferred embodiment of the present invention while still providing microelectronics fabrications formed in accord with the method of the present invention, as defined by the appended claims.

What is claimed is:

1. A method for forming a via through a dielectric layer within a microelectronics fabrication comprising:

providing a substrate employed within a microelectronics fabrication, the substrate having a contact region formed therein;

forming upon the substrate a patterned first dielectric layer, the patterned first dielectric layer defining a via accessing the contact region, the patterned first dielectric layer being formed of a first dielectric material which is not susceptible to etching with an oxygen containing plasma;

forming upon the patterned first dielectric layer a blanket second dielectric layer, the blanket second dielectric layer completely covering the patterned first dielectric layer and filling the via, the blanket second dielectric layer being formed of a second dielectric material which is susceptible to etching within the oxygen containing plasma;

forming upon the blanket second dielectric layer a blanket hard mask layer, the blanket hard mask layer being formed from a hard mask material which is not susceptible to etching within the oxygen containing plasma;

forming upon the blanket hard mask layer a patterned photoresist layer, the patterned photoresist layer leaving exposed a portion of the blanket hard mask layer greater that an areal dimension of the via and at least partially overlapping the areal dimension of the via;

etching while employing a first plasma etch method the blanket hard mask layer to form a patterned hard mask layer defining a first trench formed through the patterned hard mask layer while employing the patterned photoresist layer as a first etch mask layer, the first plasma etch method employing a first etchant gas composition to the hard mask material from which is formed the blanket hard mask layer; and

etching while employing a second plasma etch method the blanket second dielectric layer to form a patterned second dielectric layer having an aperture formed therethrough, the aperture comprising:

a second trench corresponding with the first trench; and

at least a portion of the first via, the second plasma etch method employing the oxygen containing plasma.

2. The method of claim **1** wherein the microelectronics fabrication is selected from the group consisting of semiconductor integrated circuit microelectronics fabrications, solar cell microelectronics fabrications, ceramic substrate microelectronics fabrications and flat panel display microelectronics fabrications.

3. The method of claim **1** wherein the patterned first dielectric layer is formed from a dielectric material selected from the group consisting of silicon oxide dielectric materials, silicon nitride dielectric materials and silicon oxynitride dielectric materials.

4. The method of claim **1** wherein the blanket second dielectric layer is formed from a dielectric material selected from the group consisting of organic polymer spin-on-polymer dielectric materials and amorphous carbon dielectric materials.

5. The method of claim **1** wherein there is not employed a hard mask layer interposed between the patterned first dielectric layer and the blanket second dielectric layer.

6. The method of claim **1** wherein the patterned photoresist layer is stripped from the microelectronics fabrication simultaneously with etching the blanket second dielectric layer to form the aperture through the patterned second dielectric layer.

7. A method for forming a patterned conductor layer within a microelectronics fabrication comprising:

providing a substrate employed within a microelectronics fabrication, the substrate having a contact region formed therein;

forming upon the substrate a patterned first dielectric layer, the patterned first dielectric layer defining a via accessing the contact region, the patterned first dielectric layer being formed of a first dielectric material which is not susceptible to etching with an oxygen containing plasma;

forming upon the patterned first dielectric layer a blanket second dielectric layer, the blanket second dielectric

layer completely covering the patterned first dielectric layer and filling the via, the blanket second dielectric layer being formed of a second dielectric material which is susceptible to etching within the oxygen containing plasma;

forming upon the blanket second dielectric layer a blanket hard mask layer, the blanket hard mask layer being formed from a hard mask material which is not susceptible to etching within the oxygen containing plasma;

forming upon the blanket hard mask layer a patterned photoresist layer, the patterned photoresist layer leaving exposed a portion of the blanket hard mask layer greater that an areal dimension of the via and at least partially overlapping the areal dimension of the via;

etching while employing a first plasma etch method, the blanket hard mask layer to form a patterned hard mask layer defining a first trench formed through the patterned hard mask layer while employing the patterned photoresist layer as a first etch mask layer, the first plasma etch method employing a first etchant gas composition to the hard mask material from which is formed the blanket hard mask layer;

etching,while employing a second plasma etch method the blanket second dielectric layer to form a patterned second dielectric layer having an aperture formed therethrough, the aperture comprising:

a second trench corresponding with the first trench; and

at least a portion of the first via, the second plasma etch method employing the oxygen containing plasma; and

forming into the aperture a patterned conductive stud layer.

8. The method of claim **7** wherein the microelectronics fabrication is selected from the group consisting of semiconductor integrated circuit microelectronics fabrications, solar cell microelectronics fabrications, ceramic substrate microelectronics fabrications and flat panel display microelectronics fabrications.

9. The method of claim **7** wherein the patterned first dielectric layer is formed from a dielectric material selected from the group consisting of silicon oxide dielectric materials, silicon nitride dielectric materials and silicon oxynitride dielectric materials.

10. The method of claim **7** wherein the blanket second dielectric layer is formed from a dielectric material selected from the group consisting of organic polymer spin-on-polymer dielectric materials and amorphous carbon dielectric materials.

11. The method of claim **7** wherein there is not employed a hard mask layer interposed between the patterned first dielectric layer and the blanket second dielectric layer.

12. The method of claim **7** wherein the patterned photoresist layer is stripped from the microelectronics fabrication simultaneously with etching the blanket second dielectric layer to form the aperture through the patterned second dielectric layer.

13. The method of claim **7** wherein the patterned conductive stud layer is formed employing a damascene method.

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Lin (43) **Pub. Date: Jun. 6, 2002**

(54) **TOP LAYERS OF METAL FOR HIGH PERFORMANCE IC'S**

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(22) Filed: **Jan. 29, 2002**

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Publication Classification

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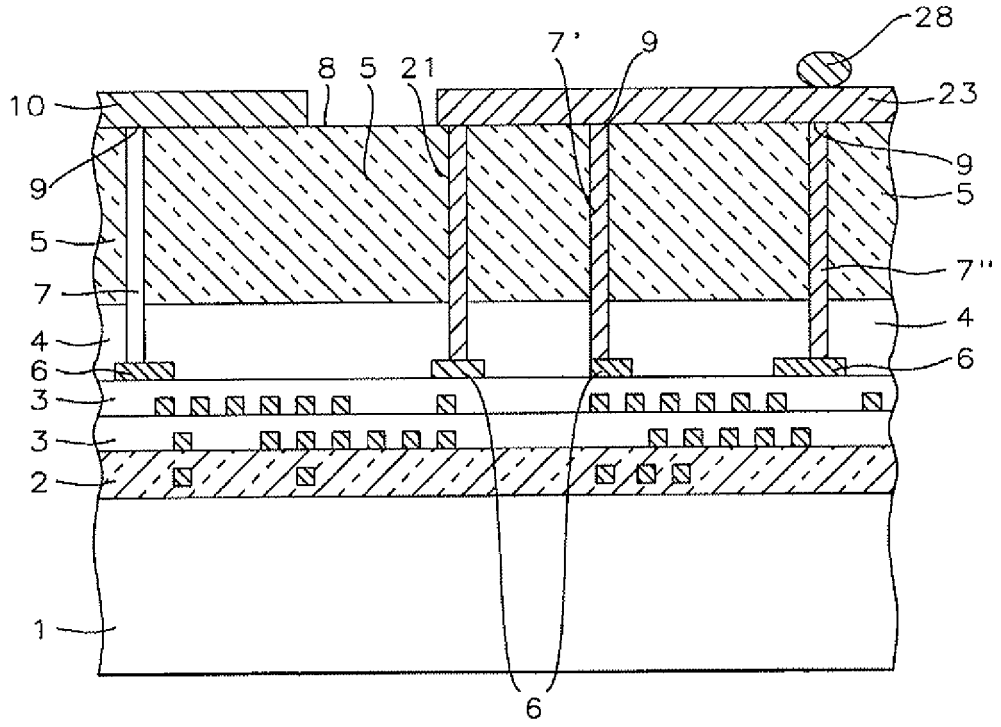
(52) **U.S. Cl.** **438/637**; 438/623; 257/758

(57) **ABSTRACT**

A method of closely interconnecting integrated circuits contained within a semiconductor wafer to electrical circuits surrounding the semiconductor wafer. Electrical interconnects are held to a minimum in length by making efficient use of polyimide or polymer as an inter-metal dielectric thus enabling the integration of very small integrated circuits within a larger circuit environment at a minimum cost in electrical circuit performance.



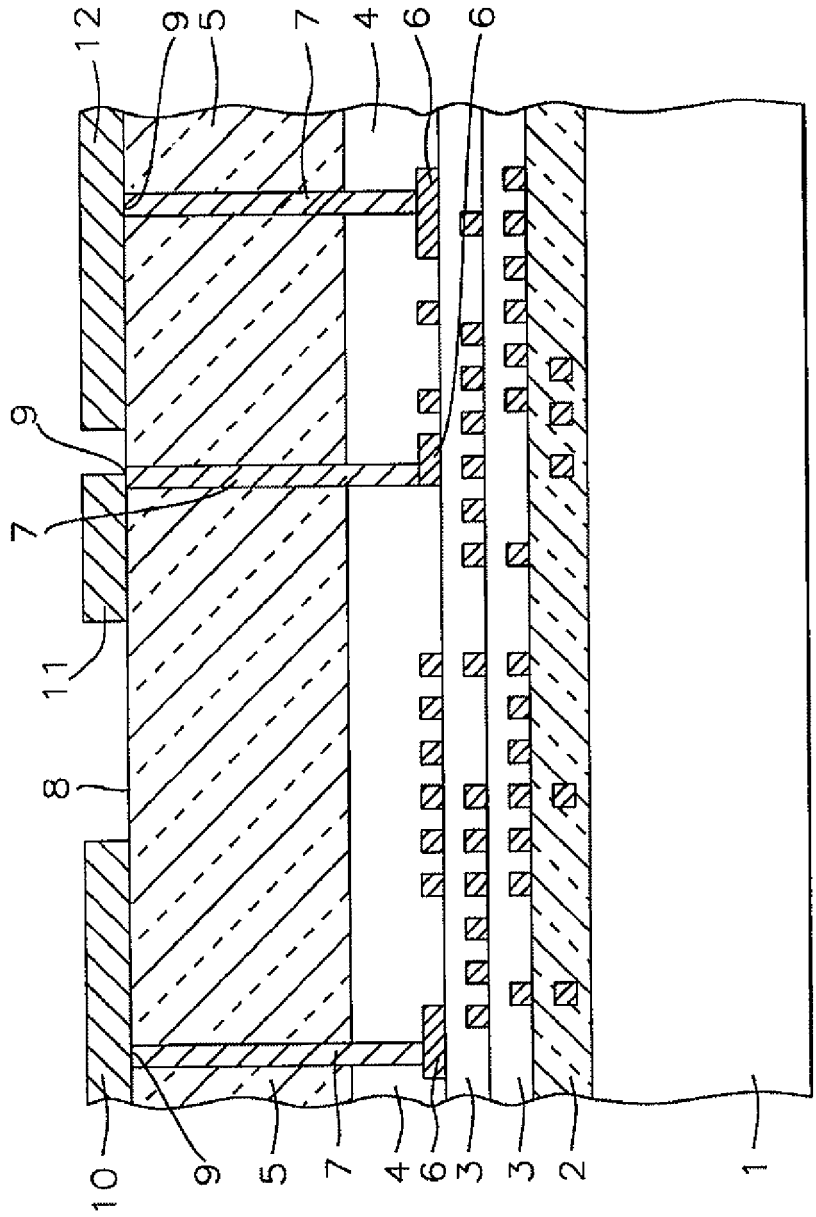


FIG. 1

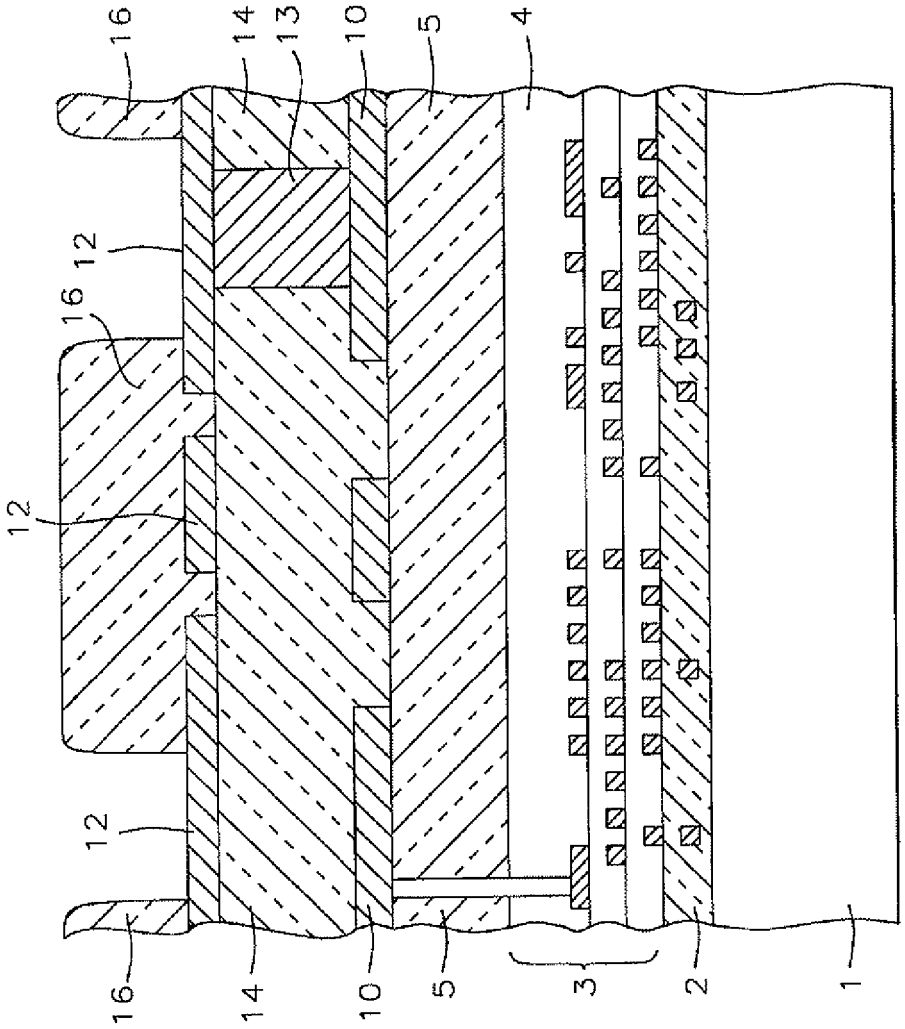


FIG. 2

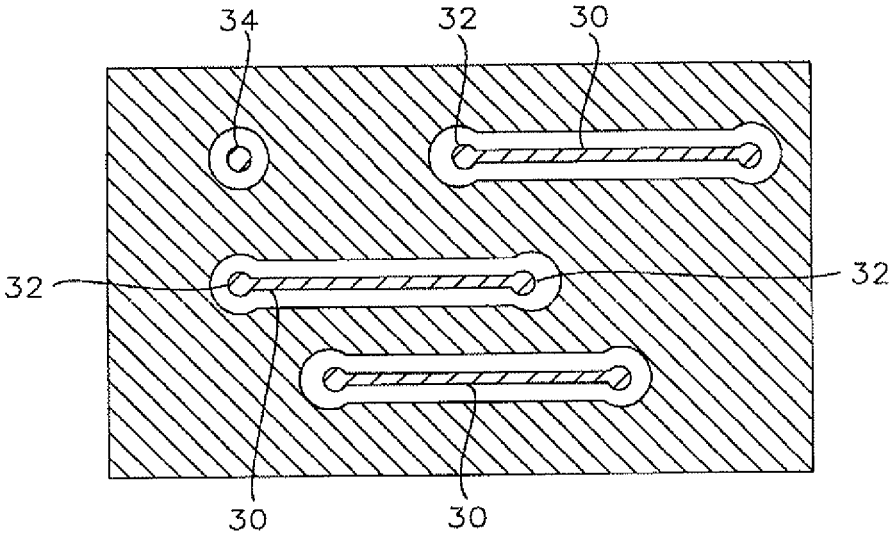


FIG. 3a

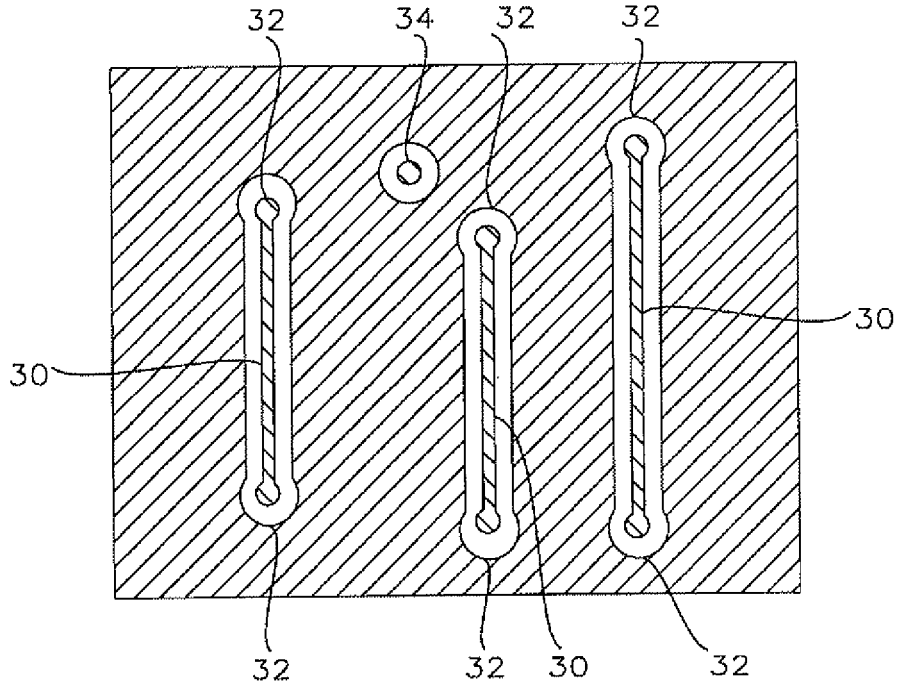


FIG. 3b

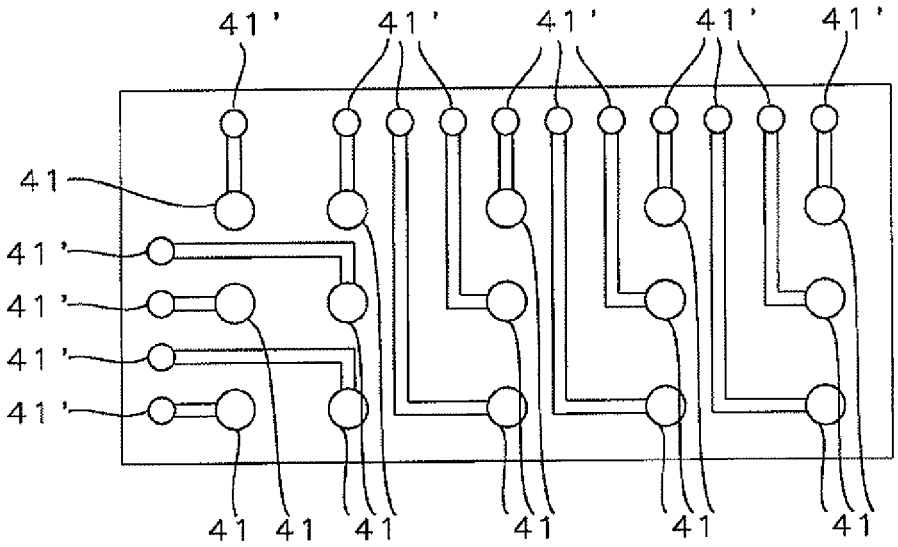


FIG. 4

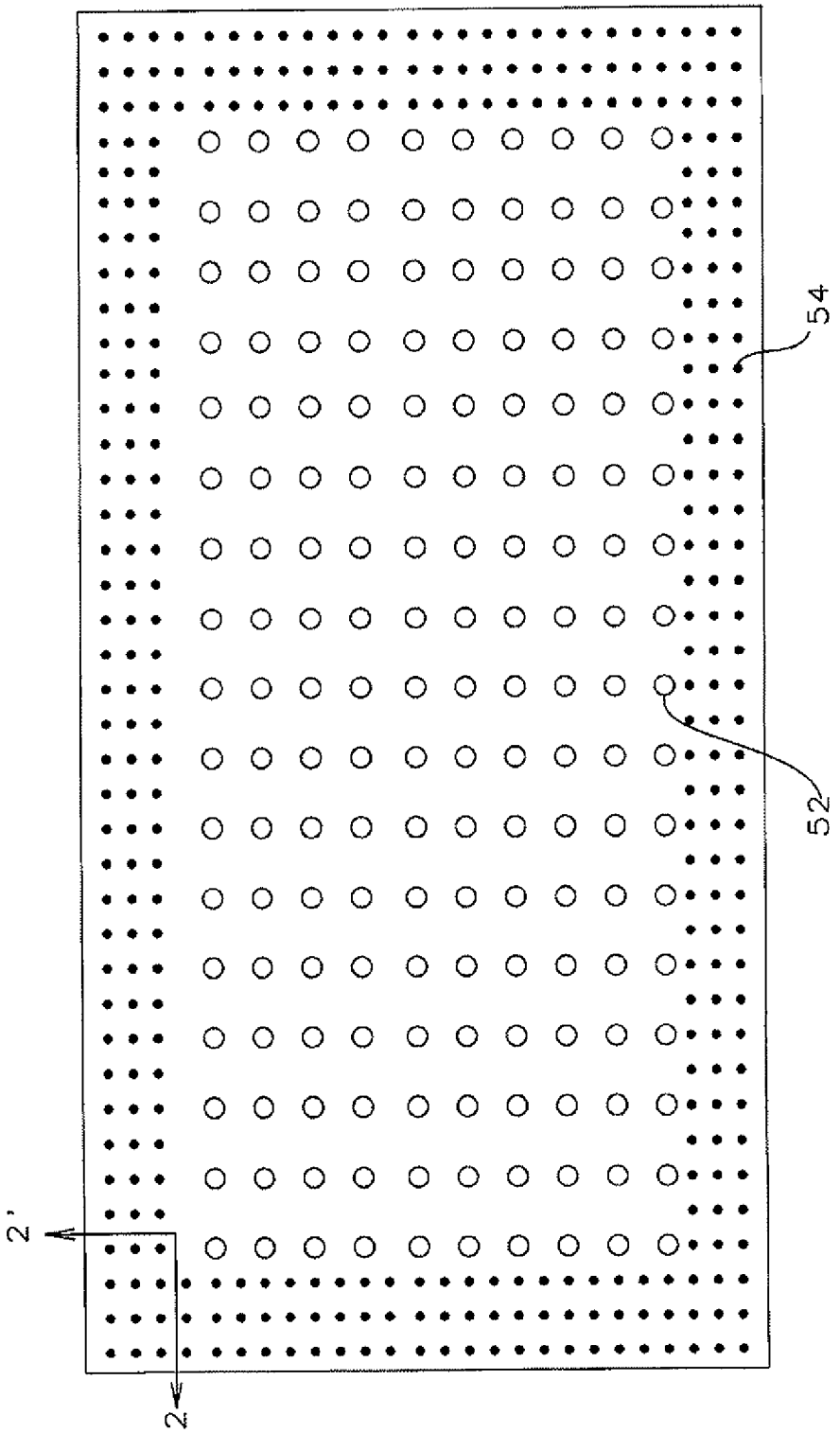


FIG. 5

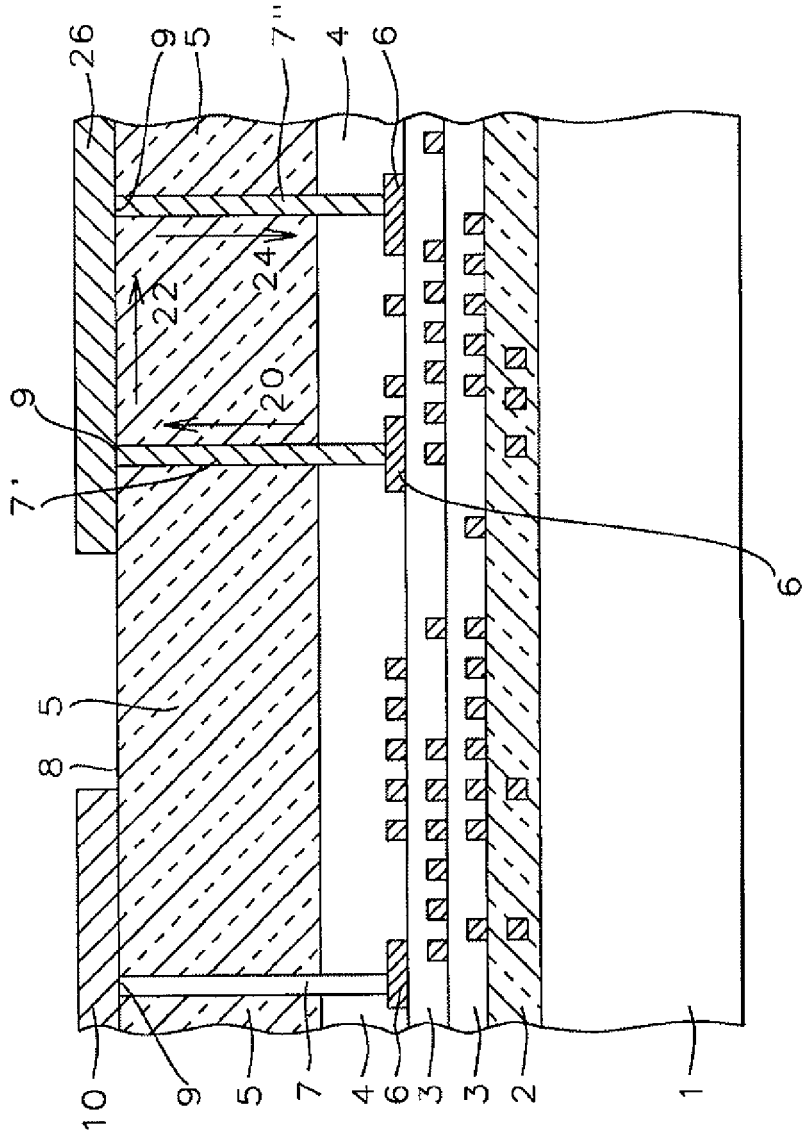


FIG. 6

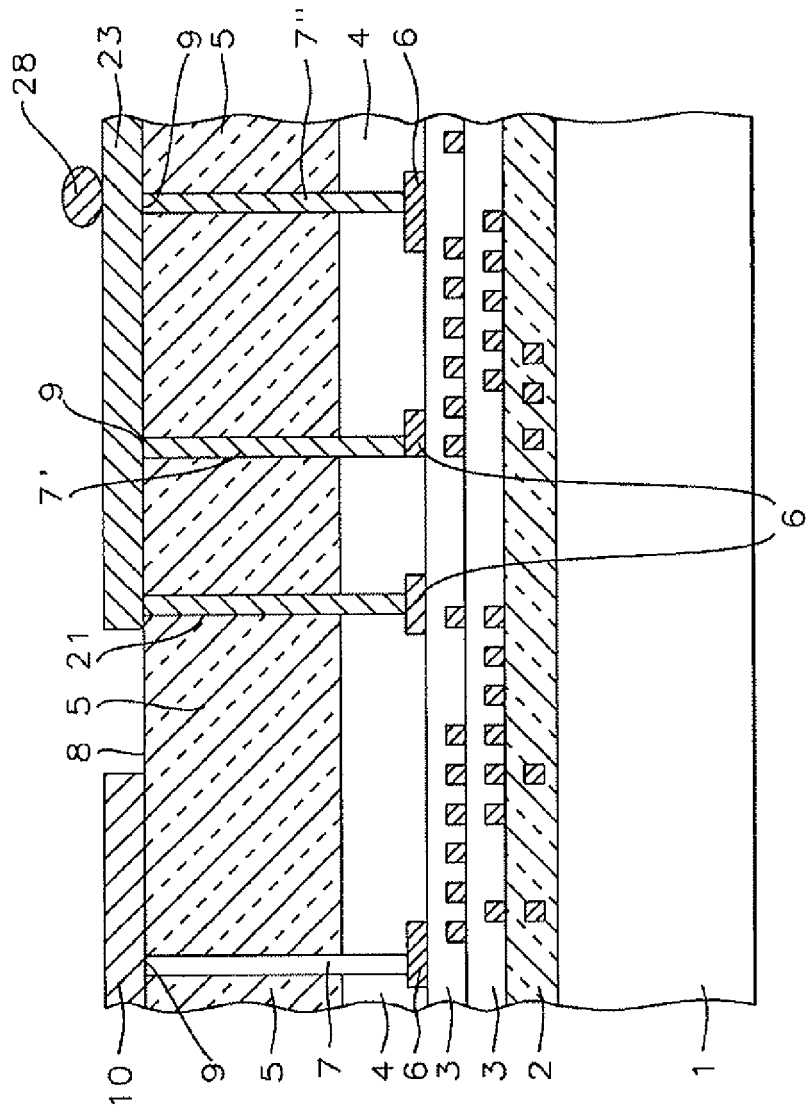


FIG. 7

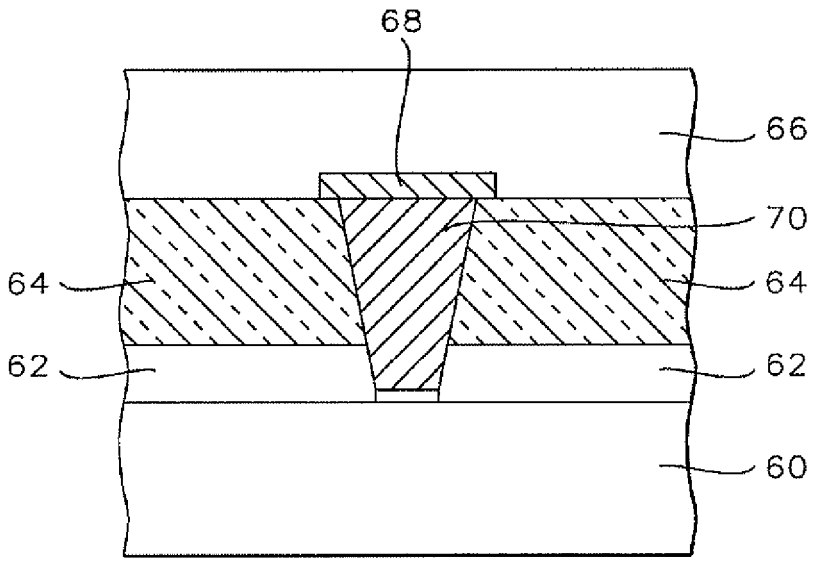

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FIG. 8

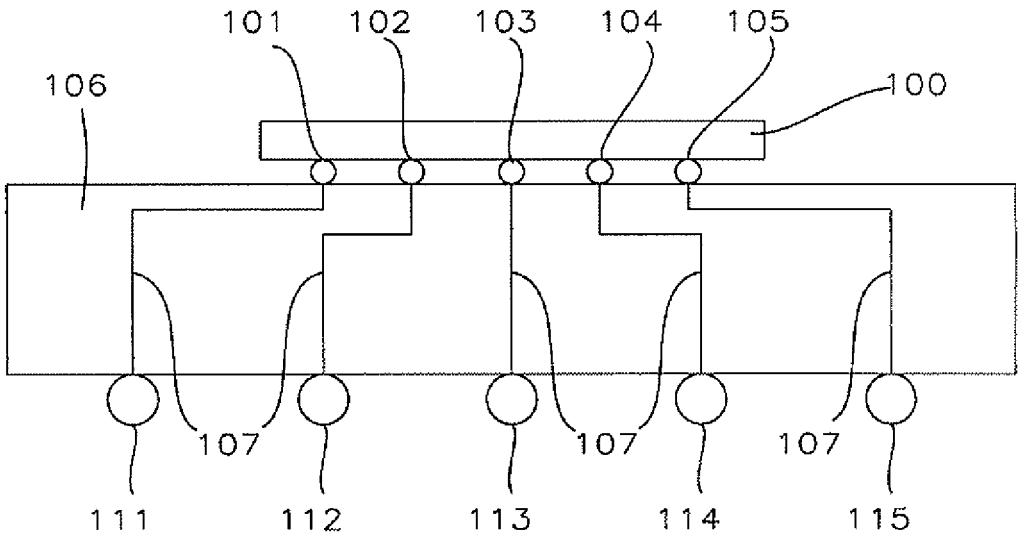
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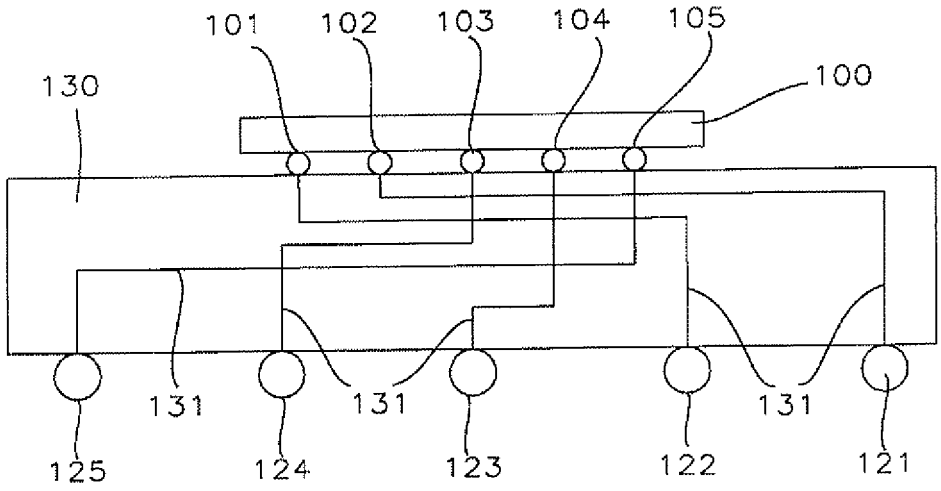
FIG. 9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121

FIG. 10

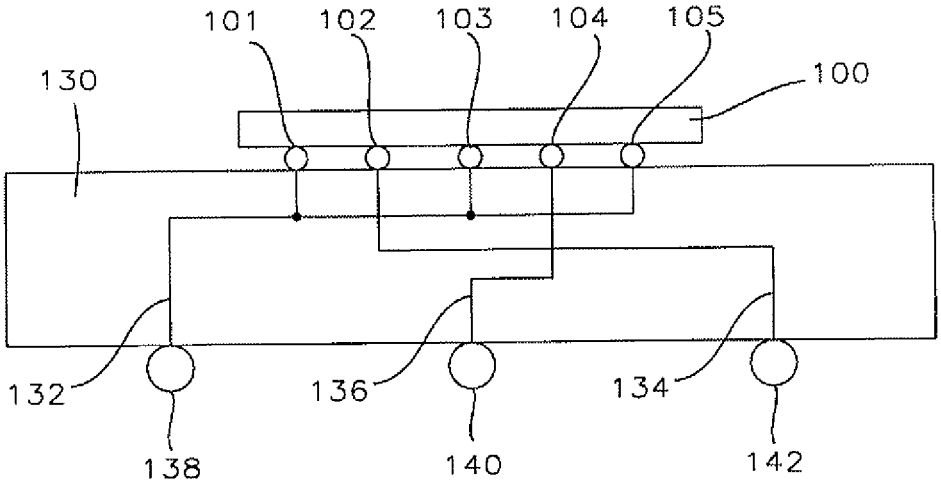
101
102
103
104
105
100
130
132
136
134
138
140
142

FIG. 11

TOP LAYERS OF METAL FOR HIGH PERFORMANCE IC'S

[0001] This application is a continuation-in-part application of Ser. No. 09/216,791, filed on Dec. 21, 1998.

BACKGROUND OF THE INVENTION

[0002] (1). Field of the Invention

[0003] The invention relates to the manufacturing of high performance Integrated Circuit (IC's), and more specifically to methods of achieving high performance of the Integrated Circuits by reducing the parasitic capacitance and resistance of interconnecting wiring on chip.

[0004] (2). Description of the Prior Art

[0005] When the geometric dimensions of the Integrated Circuits are scaled down, the cost per die is decreased while some aspects of performance are improved. The metal connections which connect the Integrated Circuit to other circuit or system components become of relative more importance and have, with the further miniaturization of the IC, an increasingly negative impact on the circuit performance. The parasitic capacitance and resistance of the metal interconnections increase, which degrades the chip performance significantly. Of most concern in this respect is the voltage drop along the power and ground buses and the RC delay of the critical signal paths. Attempts to reduce the resistance by using wider metal lines result in higher capacitance of these wires.

[0006] To solve this problem, the approach has been taken to develop low resistance metal (such as copper) for the wires while low dielectric materials are used in between signal lines.

[0007] Increased Input-Output (IO) combined with increased demands for high performance IC's has led to the development of Flip Chip Packages. Flip-chip technology fabricates bumps (typically Pb/Sn solders) on Al pads on chip and interconnect the bumps directly to the package media, which are usually ceramic or plastic based. The flip-chip is bonded face down to the package medium through the shortest path. These technologies can be applied not only to single-chip packaging, but also to higher or integrated levels of packaging in which the packages are larger and to more sophisticated substrates that accommodate several chips to form larger functional units.

[0008] The flip-chip technique, using an area array, has the advantage of achieving the highest density of interconnection to the device and a very low inductance interconnection to the package. However, pre-testability, post-bonding visual inspection, and TCE (Temperature Coefficient of Expansion) matching to avoid solder bump fatigue are still challenges. In mounting several packages together, such as surface mounting a ceramic package to a plastic board, the TCE mismatch can cause a large thermal stress on the solder-lead joints that can lead to joint breakage caused by solder fatigue from temperature cycling operations.

[0009] U.S. Pat. No. 5,212,403 (Nakanishi) shows a method of forming wiring connections both inside and outside (in a wiring substrate over the chip) for a logic circuit depending on the length of the wire connections.

[0010] U.S. Pat. No. 5,501,006 (Gehman, Jr. et al.) shows a structure with an insulating layer between the integrated circuit (IC) and the wiring substrate. A distribution lead connects the bonding pads of the IC to the bonding pads of the substrate.

[0011] U.S. Pat. No. 5,055,907 (Jacobs) discloses an extended integration semiconductor structure that allows manufacturers to integrate circuitry beyond the chip boundaries by forming a thin film multi-layer wiring decal on the support substrate and over the chip. However, this reference differs from the invention.

[0012] U.S. Pat. No. 5,106,461 (Volfson et al.) teaches a multi layer interconnect structure of alternating polyimide (dielectric) and metal layers over an IC in a TAB structure.

[0013] U.S. Pat. No. 5,635,767 (Wenzel et al.) teaches a method for reducing RC delay by a PBGA that separates multiple metal layers.

[0014] U.S. Pat. No. 5,686,764 (Fulcher) shows a flip chip substrate that reduces RC delay by separating the power and I/O traces.

SUMMARY OF THE INVENTION

[0015] It is the primary objective of the present invention is to improve the performance of High Performance Integrated Circuits.

[0016] Another objective of the present invention is to reduce resistive voltage drop of the power supply lines that connect the IC to surrounding circuitry or circuit components.

[0017] Another objective of the present invention is to reduce the RC delay constant of the signal paths of high performance IC's.

[0018] Yet another objective of the present invention is to facilitate the application of IC's of reduced size and increased circuit density.

[0019] Yet another objective of the present invention is to further facilitate and enhance the application of low resistor conductor metals.

[0020] Yet another objective of the present invention is to allow for increased I/O pin count for the use of high performance IC's.

[0021] Yet another objective of the present invention is to simplify chip assembly by reducing the need for re-distribution of I/O chip connections.

[0022] Yet another objective of the present invention is to facilitate the connection of high-performance IC's to power buses.

[0023] Yet another objective of the present invention is to facilitate the connection of high-performance IC's to clock distribution networks.

[0024] Yet another objective of the present invention is to reduce IC manufacturing costs by allowing or facilitating the use of less expensive process equipment and by accommodating less strict application of clean room requirements, this as compared to sub-micron manufacturing requirements.

[0025] Yet another objective of the present invention is to be a driving force and stimulus for future system-on-chip designs since the present invention allows ready and cost

effective interconnection between functional circuits that are positioned at relatively large distances from each other on the chip.

[0026] Yet another objective of the present design is to form the basis for a computer based routing tool that automatically routes interconnections that exceed a predetermined length in accordance with the type of interconnection that needs to be established.

[0027] The present invention adds one or more thick layers of dielectric and one or more layers of wide metal lines on top of the finished device wafer. The thick layer of dielectric can, for example, be of polyimide or benzocyclobutene (BCB) with a thickness of over, for example, 3 um. The wide metal lines can, for instance, be of aluminum or electroplated copper. These layers of dielectric and metal lines can be used for power buses or power planes, clock distribution networks, critical signal, re-distribution of I/O pads for flip chip applications, and for long signal paths.

BRIEF DESCRIPTION OF THE DRAWINGS

[0028] **FIG. 1** shows a cross section of the interconnection scheme of the present invention.

[0029] **FIG. 2** shows a cross section of the present invention in a more complex circuit configuration.

[0030] **FIG. 3***a* shows the top view of a combination power and X-signal plane using the present invention.

[0031] **FIG. 3***b* shows the top view of a combination power and Y-signal plane using the present invention.

[0032] **FIG. 4** shows the top view of solder bump arrangement using the present invention and is an expanded view of a portion of **FIG. 5**.

[0033] **FIG. 5** shows the top view of an example of power/ground pads combined with signal pad using the present invention.

[0034] **FIG. 6** shows a basic integrated circuit (IC) interconnect scheme of the invention.

[0035] **FIG. 7** shows an extension of the basic IC interconnect scheme by adding power, ground and signal distribution capabilities.

[0036] **FIG. 8** shows an approach of how to transition from sub-micron metal to wide metal interconnects.

[0037] **FIG. 9** shows detail regarding BGA device fan out using the invention.

[0038] **FIG. 10** shows detail regarding BGA device pad relocation using the invention.

[0039] **FIG. 11** shows detail regarding the usage of common power, ground and signal pads for BGA devices using the invention.

DETAILED DESCRIPTION OF THE INVENTION

[0040] The present invention teaches an Integrated Circuit structure where key re-distribution and interconnection metal layers and dielectric layers are added over a conventional IC. These re-distribution and interconnection layers allow for wider buses and reduce conventional RC delay.

[0041] Referring now more specifically to **FIG. 1**, there is shown a cross section of one implementation of the present invention. A silicon substrate **1** has transistors and other devices, typically formed of poly silicon, covered by a dielectric layer **2** deposited over the devices and the substrate. Layer **3** indicates the totality of metal layers and dielectric layers that are typically created on top of the device layer **2**. Points of contact **6**, such as bonding pads known in the semiconductor art, are in the top surface of layers **3** and are part of layer **3**. These points of contact **6** are points within the IC arrangement that need to be further connected to surrounding circuitry, that is to power lines or to signal lines. A passivation layer **4**, formed of for example silicon nitride, is deposited on top of layer **3**, as is known in the art for protecting underlying layers from moisture, contamination, etc.

[0042] The key steps of the invention begin with the deposition of a thick layer **5** of polyimide is deposited. A pattern **7** is exposed and etched through the polyimide layer **5** and the passivation layer **4** where the pattern **7** is the same as the pattern of the contact points **6**. This opens the contact points **6** up to the surface **8** of the polyimide layer **5**.

[0043] Electrical contact with the contact points **6** can now be established by filling the openings **7** with a conductor. The tops **9** of this metal conductor can now be used for connection of the IC to its environment, and for further integration into the surrounding electrical circuitry. Pads **10**, **11** and **12** are formed on top of the top **9** of the metal conductors **7**; these pads can be of any design in width and thickness to accommodate specific circuit design requirements. A larger size pad can, for instance, be used as a flip chip pad. A somewhat smaller in size pad can be used for power distribution or as a ground or signal bus. The following connections can, for instance, be made to the pads shown in **FIG. 1**: pad **10** can serve as a flip chip pad, pad **11** can serve as a flip chip pad or can be connected to electrical power or to electrical ground or to an electrical signal bus, pad **12** can also serve as a flip chip pad. There is no connection between the size of the pads shown in **FIG. 1** and the suggested possible electrical connections for which this pad can be used. Pad size and the standard rules and restrictions of electrical circuit design determine the electrical connections to which a given pad lends itself.

[0044] The following comments relate to the size and the number of the contact points **6**, **FIG. 1**. Because these contact points **6** are located on top of a thin dielectric (layer **3**, **FIG. 1**) the pad size cannot be too large since a large pad size brings with it a large capacitance. In addition, a large pad size will interfere with the routing capability of that layer of metal. It is therefore preferred to keep the size of the pad **6** small. The size of pad **6** is however also directly related with the aspect ratio of via **7**. An aspect ratio of about **5** is acceptable for the consideration of via etching and via filling. Based on these considerations, the size of the contact pad **6** can be in the order of 0.5 um. to 3 um. the exact size being dependent on the thickness of layers **4** and **5**.

[0045] The present invention does not impose a limitation on the number of contact pads that can be included in the design; this number is dependent on package design requirements. Layer **4** in **FIG. 1** can be a typical IC passivation layer.

[0046] The most frequently used passivation layer in the present state of the art is plasma enhanced CVD (PECVD)

oxide and nitride. In creating layer **4**, a layer of approximately 0.2 um. PECVD oxide is deposited first followed by a layer of approximately 0.7 um. nitride. Passivation layer **4** is very important because it protects the device wafer from moisture and foreign ion contamination. The positioning of this layer between the sub-micron process (of the integrated circuit) and the tens-micron process (of the interconnecting metalization structure) is of critical importance since it allows for a cheaper process that possibly has less stringent clean room requirements for the process of creating the interconnecting metalization structure.

[0047] Layer **5** is a thick polymer dielectric layer (for example polyimide) that have a thickness in excess of 2 um (after curing). The range of polyimide thickness can vary from 2 um. to 30 um. dependent on electrical design requirements.

[0048] For the deposition of layer **5** the Hitachi-Dupont polyimide HD 2732 or 2734 can, for example, be used. The polyimide can be spin-on coated and cured. After spin-on coating, the polyimide will be cured at 400 degrees C. for 1 hour in a vacuum or nitrogen ambient. For thicker polyimide, the polyimide film can be multiple coated and cured.

[0049] Another material that can be used to create layer **5** is the polymer benzocyclobutene (BCB). This polymer is at this time commercially produced by for instance Dow Chemical and has recently gained acceptance to be used instead of typical polyimide application.

[0050] The dimensions of opening **7** have previously been discussed. The dimension of the opening together with the dielectric thickness determine the aspect ratio of the opening. The aspect ratio challenges the via etch process and the metal filling capability. This leads to a diameter for opening **7** in the range of approximately 0.5 um. to 3.0 um. while the height for opening **7** can be in the range of approximately 3 um. to 20 um. The aspect ratio of opening **7** is designed such that filling of the via with metal can be accomplished. The via can be filled with CVD metal such as CVD tungsten or CVD copper, with electro-less nickel, with a damascene metal filling process, with electroplating copper, etc.

[0051] It must be noted that the use of polyimide films as inter-level dielectrics has been pursued as a technique for providing partial planarization of a dielectric surface. Polyimides offer the following characteristics for such applications:

[0052] they produce surfaces in which the step heights of underlying features are reduced, and step slopes are gentle and smooth.

[0053] they are available to fill small openings without producing the voids that occur when low-temperature CVD oxide films are deposited.

[0054] the cured polyimide films can tolerate temperatures of up to 500 degrees C. without degradation of their dielectric film characteristics.

[0055] polyimide films have dielectric breakdowns, which are only slightly lower than that of SiO_2.

[0056] the dielectric constant of polyimides is smaller than that of silicon nitride and of SiO_2.

[0057] the process used to deposit and pattern polyimide films is relatively simple.

[0058] For all of the above characteristics, polyimides are used and recommended within the scope of the present invention.

[0059] **FIG. 2** shows how the present invention as indicated in **FIG. 1** can be further extended to include multiple layers of polyimide and, in so doing, can be adapted to a larger variety of applications. The lower level build up of this cross section is identical to the build up shown in **FIG. 1** with a silicon wafer **1**, the poly silicon layer **2**, the metal and dielectric combined layer **3**, the passivation layer **4**, the polyimide layer **5** and the pads **10** deposited on top of layer **5**. The function of the structure that has been described in **FIG. 1** can be further extended by depositing another layer of polyimide **14** on top of the previously deposited layer **5** and overlaying the pads **10**. Selective etching and metal deposition can further create contact points **12**. These contact points **12** can be connected with pads **10** as shown by connector **13**. Depositing pads **12** on top of layer **14** can thus further extend this process. These pads **12** can be further customized to a particular application, the indicated extension of multiple layers of polyimides greatly enhances the flexibility and usefulness of the present invention. Additional alternating layers of polyimide and metal lines and/or power or ground planes may be added above layers **12** and **16**, as needed.

[0060] **FIGS. 3*a*** and **3*b*** show a top view of one possible use of the present invention. Interconnecting a number of pads **32** that have been created as described creates signal lines **30**. Additional contact points such as point **34** can allow signal lines to pass vertically between layers. The various contact points can, for instance, be created within the surface of a power plane or ground plane **36**. The layers within the interconnecting metalization structure of the present invention can contain signal interconnections in the X-direction, signal interconnections in the Y-direction, signal interconnections between X and or Y directions, interconnections to and/or within power and/or ground buses. The present invention further teaches the interconnection of signal lines, power and ground buses between the connected IC's and the top of the metalization system of the present invention.

[0061] **FIG. 3*a*** shows signal lines formed in the X-direction, **FIG. 3*b*** shows signal lines formed in the Y-direction.

[0062] **FIG. 4** presents yet another application of the present invention. Shown in **FIG. 4** is an exploded view of a part of **FIG. 5** that presents an area array I/O distribution. **FIG. 4** shows pads **41** (on which solder bumps can be created) and an example of a layout of the redistribution of the peripheral pads **41'**. The exploded view of **FIG. 4** is taken along the line **2-2'** shown in **FIG. 5**, the redistribution of the peripheral pads **41'** (see **FIG. 4**) is, for clarity of overview, not shown in **FIG. 5**. The power or ground connections can be made to any point that is required on the bottom device. Furthermore, the power and ground planes can be connected to the power and ground planes of the package substrates. **FIG. 4** shows an example of how to use the topmost metal layer to redistribute the peripheral pads **41'** to become area array pads **41**. The solder bumps can then be created on pads **41**.

[0063] **FIG. 5** shows the top surface of a plane that contains a design pattern of a combination of power or ground pads **52** and signal pads **54**. **FIG. 5** shows the pad

openings in the top dielectric layer. It is to be noted that the ground/power pads **52** are heavier and larger in design relative to the signal pads **54**. The present invention ideally lends itself to meeting these differences in design, as they are required within the art of chip and high performance circuit design. The number of power or ground pads **52** shown in **FIG. 5** can be reduced is there are power and/or ground planes within the chip. From this it is clear that the package number of I/O's can be reduced within the scope of the present invention which leads to a reduction of the package cost by eliminating common signal/power/ground connections within the package. For instance, a 470 I/O count on a BGA chip can, within the scope of the present invention, be reduced to a 256 I/O count using the present invention. This results in considerable savings for the overall package.

[0064] **FIG. 6** shows a basic design advantage of the invention. This advantage allows for the sub-micron or fine-lines, that run in the immediate vicinity of the metal layers **3** and the contact points **6**, to be extended in an upward direction **20** through metal interconnect **7'**, this extension continues in the direction **22** in the horizontal plane of the metal interconnect **26** and comes back down in the downward direction **24** through metal interconnect **7"**. The functions and constructs of the passivation layer **4** and the insulating layer **5** remain as previously highlighted under **FIG. 1**. This basic design advantage of the invention is to "elevate" or "fan-out" the fine-line interconnects and to remove these interconnects from the micro and sub-micro level to a metal interconnect level that has considerably larger dimensions and is therefore with smaller resistance and capacitance and is easier and more cost effectively to manufacture. This aspect of the invention does not include any aspect of conducting line redistribution and therefore has an inherent quality of simplicity. It therefore further adds to the importance of the invention in that it makes micro and sub-micro wiring accessible at a wide-metal level. The interconnections **7'** and **7"** interconnect the fine-level metal by going up through the passivation and polymer or polyimide dielectric layers, transverses over a distance on the wide-metal level and continues by descending from the wide-metal level back down to the fine-metal level by again transversing down through the passivation and polymer or polyimide dielectric layers. The extensions that are in this manner accomplished need not to be limited to extending fine-metal interconnect points **6** of any particular type, such as signal or power or ground, with wide metal line **26**. The laws of physics and electronics will impose limitations, if any, as to what type of interconnect can by established in this manner where limiting factors will be the conventional limiting factors of resistance, propagation delay, RC constants and others. Where the invention is of importance is that the invention provides much broader latitude in being able to apply these laws and, in so doing, provides a considerably extended scope of the application and use of Integrated Circuits and the adaptation of these circuits to a wide-metal environment.

[0065] **FIG. 7** shows how the basic interconnect aspect of the invention can further be extended to now not only elevate the fine-metal to the plane of the wide-metal but to also add power, ground and signal distribution interconnects of power, ground and signal planes at the wide-metal level. The wide-metal interconnect **26** of **FIG. 6** is now extended to further include an interconnection with the via **21**. In typical IC design, some pads may not be positioned in a location from which easy fan-out can be accomplished to a location that is required for the next step of circuit assembly. In those cases, the BGA substrate requires additional layers in the package construction in order to accomplish the required fan-out. The invention teaches an approach that makes additional layers in the assembling of an IC feasible while not unduly increasing the cost of creating such a multi-layer interface. Ball formation **28** on the surface of interconnect **23** indicates how the invention replaces part of the conventional BGA interconnect function, the solder bump provides for flip chip assembly. This interconnect **28** now connects the BGA device with surrounding circuitry at the wide-metal level as opposed to previous interconnects of the BGA device at the fine-metal level. The wide-metal interconnect of the BGA has obvious advantages of cost of manufacturing and improved BGA device performance. By being able to readily extend the wide-metal dimensions it also becomes possible to interconnect power, ground and signal lines at a wide-metal level thereby reducing the cost and complexity of performing this function at the fine-metal level. The indication of **28** as a ball does not imply that the invention is limited to solder bumps for making interconnects. The invention is equally applicable to wirebonding for making circuit interconnects.

[0066] **FIG. 8** further shows a cross section wherein the previous linear construction of the metal interconnection running through the passivation layer and the insulation layer is now conical in form. The sub-micron metal layer **60** is covered with a passivation layer **62**, a layer **64** of polyimide or polymer is deposited over the passivation layer **62**. The wide metal level **66** is formed on the surface of layer **64**. The via **70** is shown as having sloping sides, these sloping sides can be achieved by controlling the photolithography process that is used to created the via **70**. The etching of the polyimide or polymer can for instance be done under an angle of about 75 degrees with the following curing being done under an angle of 45 degrees. Also, a photosensitive polyimide or polymer can be used, the cone shape of the via **70** can in that case be achieved by variation of exposure combined with time of exposure combined with angle of exposure. Where non-photosensitive polymer or polyimide is used, a wet etch can be applied that has a gradated faster and longer time etch as the top of the via **70** is being approached. The layer of wide-metal pad **68** is deposited on the surface of the polymer or polyimide layer **64**, the wide-metal pad deposition **68** mates with the top surface of the via **70** and is centered on top of this surface.

[0067] **FIGS. 9 through 11** show further detail to demonstrate the concepts of BGA chip ball fan-out, pad relocation and the creation of common ground, power and signal pads.

[0068] **FIG. 9** shows a cross section **100** of a BGA chip, five balls **101** through **105** are also shown. By using the BGA substrate **106** and the wiring **107** within the substrate **106**, it is clear that ball **101** can be repositioned to location **111**, ball **102** to location **112**, etc. for the remaining solder bumps **103** through **105**. It is clear that the separation of contact points **111** through **115** is considerably larger than the separation of the original solder bumps **101** through **105**. The BGA substrate **106** is the subject of the invention, this substrate allows for spreading the distance between the contact points or balls of the BGA device to a considerable degree.

[0069] **FIG. 10** shows the concept of pad relocation. BGA pad **120** can be any of the contact balls **101** through **105**. By using the BGA substrate **130** and the wiring **131** that is provided within the substrate, it is clear that the BGA pads can be arranged in a different and arbitrary sequence that is required for further circuit design or packaging. For instance contact point **101**, which is on the far left side of the BGA device **100**, is re-routed to location **121** which is on the second far right of the BGA substrate **130**. The re-arrangements of the other BGA solder bumps can readily be learned from following the wiring **130** within the substrate **131** and by tracing from solder bump to one of the contact points **122** through **125** of the BGA substrate.

[0070] **FIG. 11** shows the interconnecting of BGA device solder bumps into common power, ground or signal pads. The BGA chip **100** is again shown with five solder bumps **101** through **105**. The BGA substrate **130** contains a wiring scheme that contains in this example three wiring units, one for each for the power, ground and signal bumps of the BGA device. It is clear from **FIG. 11** that wire arrangement **132** connects BGA device solder bumps **101**, **103** and **105** to interconnect point **138** of the BGA substrate **130**. It can further be seen that BGA device solder bump **104** is connected to interconnect point **140** of the BGA substrate by means of the wire arrangement **136**, while BGA device solder bump **102** is connected to interconnect point **142** of the BGA substrate by means of the wire arrangement **134**. The number of pins required to interconnect the BGA device **100** is in this manner reduced from five to three. It is clear that for more BGA device solder bumps, as is the case for an actual BGA device, the numeric effect of the indicated wiring arrangement is considerably more beneficial.

[0071] Some of the advantages of the present invention are:

[0072] 1) improved speed of the IC interconnections due to the use of wider metal lines (which results in lower resistance) and thicker dielectrics between the interconnecting lines (which results in lower capacitance and reduced RC delay). The improved speed of the IC interconnections results in improved performance of High Performance IC's.

[0073] 2) an inexpensive manufacturing process since there is no need for expensive equipment that is typically used in sub-micron IC fabrication; there is also no need for the extreme clean room facilities that are typically required for sub-micron manufacturing.

[0074] 3) reduced packaging costs due to the elimination of the need for redundant I/O and multiple power and ground connection points that are needed in a typical IC packaging.

[0075] 4) IC's of reduced size can be packaged and inter-connected with other circuit or system components without limiting the performance of the IC's.

[0076] 5) since dependence on ultra-fine wiring is reduced, the use of low resistance conductor wires is facilitated.

[0077] 6) structures containing more complicated IC's can be created because the invention allows for increased I/O pin count.

[0078] 7) more complicated IC's can be created without the need for a significant increase in re-distribution of package I/O connections.

[0079] 8) power buses and clock distribution networks are easier to integrate within the design of IC's.

[0080] 9) future system-on-chip designs will benefit from the present invention since it allows ready and cost effective interconnection between functional circuits that are positioned at relatively large distances from each other on the chip.

[0081] 10) form the basis for a computer based routing tool that automatically routes interconnections that exceed a predetermined length in accordance with the type of interconnection that needs to be established.

[0082] 11) provide a means to standardize BGA packaging.

[0083] 12) be applicable to both solder bumps and wirebonding for making further circuit interconnects.

[0084] 13) provide a means for BGA device solder bump fan-out thereby facilitating the packing and design of BGA devices.

[0085] 14) provide a means for BGA device pad relocation thereby providing increased flexibility for the packing and design of BGA devices.

[0086] 15) provide a means for common BGA device power, ground and signal lines thereby reducing the number of pins required to interconnect the BGA device with the surrounding circuits.

[0087] 16) provide a means for more relaxed design rules in designing circuit vias by the application of sloped vias.

[0088] 17) provide the means for extending a fine-wire interconnect scheme to a wide-wire interconnect scheme without the need to apply a passivation layer over the surface of the fine-wire structure.

[0089] Although the preferred embodiment of the present invention has been illustrated, and that form has been described in detail, it will be readily understood by those skilled in the art that various modifications may be made therein without departing from the spirit of the invention or from the scope of the appended claims.

What is claimed is:

1. A method for forming a top metalization system for high performance integrated circuits, comprising:

forming an integrated circuit comprising a plurality of devices formed in and on a semiconductor substrate, with an overlaying interconnecting metalization structure connected to said devices and comprising a plurality of first metal lines in one or more layers;

depositing a passivation layer over said interconnecting metalization structure;

depositing an insulating, separating layer over said passivation layer that is substantially thicker than said passivation layer;

forming openings through said insulating, separating layer and said passivation layer to expose upper metal portions of said overlaying interconnecting metalization structure;

depositing metal contacts in said openings; and

forming said top metalization system connected to said overlaying interconnecting metalization structure, wherein said top metalization system comprises a plurality of top metal lines, in one or more layers, each of said top metal lines having a width substantially greater than said first metal lines.

2. The method of claim 1 wherein the top metalization system connects portions of said interconnecting metalization structure to other portions of said interconnecting metalization structure.

3. The method of claim 1 wherein said top metalization system comprises signal lines that are substantially wider than lines in said interconnecting metalization structure.

4. The method of claim 1 wherein said top metalization system comprises power planes having power buses that are substantially wider than lines in said interconnecting metalization structure.

5. The method of claim 1 wherein said top metalization system comprises ground planes having ground buses that are substantially wider than lines in said interconnecting metalization structure.

6. The method of claim 1 wherein said top metalization system comprises planes that contain both signal lines and power buses that are substantially wider than lines in said interconnecting metalization structure.

7. The method of claim 1 wherein said top metalization system comprises planes that contain both signal lines and ground buses that are substantially wider than lines in said interconnecting metalization structure.

8. The method of claim 1 wherein said top metalization system comprises planes that contain both power buses and ground buses that are substantially wider than lines in said interconnecting metalization structure.

9. The method of claim 1 wherein said overlaying interconnecting metalization structure comprises electrical contact points.

10. The method of claim 9 wherein the size of said contact points is within the range of approximately 0.3 um. to 5.0 um.

11. The method of claim 1 wherein said passivation layer comprises Plasma Enhanced CVD (PECVD) oxide.

12. The method of claim 1 wherein said passivation layer comprises Plasma Enhanced CVD (PECVD) nitride.

13. The method of claim 1 wherein said passivation layer comprises a layer within the range of approximately 0.15 to 2.0 um of Plasma Enhanced CVD (PECVD) oxide over which a layer within the range of approximately 0.5 to 2.0 um PECVD nitride is deposited.

14. The method of claim 1 wherein said insulating, separating layer is a polymer dielectric layer or any other appropriate insulating material.

15. The method of claim 1 wherein said insulating, separating layer comprises polyimide.

16. The method of claim 1 wherein said insulating, separating layer comprises the polymer benzocyclobutene (BCB).

17. The method of claim 1 wherein said insulating, separating layer is of a thickness after curing within the range of approximately 1.0 to 30 um.

18. The method of claim 1 wherein said insulating, separating layer is spin-on coated and cured.

19. The method of claim 1 wherein said insulating, separating layer after said spin-on coating is cured at a temperature within the range of approximately 250 to 450 degrees C. for a time within the range of approximately 0.5 to 1.5 hours said curing to occur within a vacuum or nitrogen ambient.

20. The method of claim 16 wherein said insulating, separating layer is subjected to multiple processing steps of spin on coating and curing.

21. The method of claim 20 wherein said insulating, separating layer after each process step of said spin on coating is cured at a temperature within the range of approximately 250 to 450 degrees C. for a time within the range of approximately 0.5 to 1.5 hours said curing the occur within a vacuum or nitrogen ambient.

22. The method of claim 1 wherein said openings have an aspect ratio within the range of approximately 1 to 10.

23. The method of claim 1 wherein said metal contacts are selected from a group comprise sputtered aluminum, CVD tungsten, CVD copper, electroplated copper and electroless nickel.

24. The method of claim 1 wherein said metal contacts comprise damascene metal filling.

25. The method of claim 1 wherein said top metalization system comprises contact pads on the top metal layer whereby said contact pad can comprise any appropriate contact material, such as but not limited to tungsten, chromium, copper (electroplated or electroless), aluminum, polysilicon, or the like.

26. The method of claim 1 wherein said top metal layer comprises contact pads, said contact pads comprising signal connection pads whereby said signal connection pads can comprise any appropriate contact material, such as but not limited to tungsten, chromium, copper (electroplated or electroless), aluminum, polysilicon, or the like.

27. The method of claim 1 wherein said top metalization system contains contact pads on the top metal layer, said contact pads containing signal connection pads in addition to power and ground connection pads whereby said signal connection pads can comprise any appropriate contact material, such as but not limited to tungsten, chromium, copper (electroplated or electroless), aluminum, polysilicon, or the like.

28. The method of claim 27 wherein said signal pads are mounted in the periphery of said top metalization system and said power and ground connection pads are mounted within the area enclosed by said signal pads whereby said power and ground connection pads and said signal pads can comprise any appropriate contact material, such as but not limited to tungsten, chromium, copper (electroplated or electroless), aluminum, polysilicon, or the like.

29. A semiconductor device structure comprising:

a semiconductor substrate comprising semiconductor devices; an interconnecting metalization structure connected to said devices;

electrical contact points on an upper top surface of said interconnecting metalization structure and connected to said interconnecting metalization structure;

a passivation layer deposited over said interconnecting metalization structure and over said electrical contact points;

an insulating layer deposited over said passivation layer said insulating layer being substantially thicker than said passivation layer;

openings through said insulating layer and through said passivation layer down to the upper surface of said electrical contact points;

metal conductors within said openings; and

an upper metalization structure connected to said metal conductors.

30. The method of claim 29 wherein the upper metalization structure connects portions of said interconnecting metalization structure to other portions of said interconnecting metalization structure.

31. The structure of claim 29 wherein said upper metalization structure further comprises:

a plurality of insulating layers;

a plurality of structures of metal interconnecting lines formed between said insulating layers;

a plurality of contact pads in an upper layer of said metalization structure; and

a plurality of filled openings connecting said contact pads with one or more of said structures of metal interconnecting lines further connecting said contact pads with said electrical contact points.

32. The structure of claim 31 whereby said metal interconnecting lines are signal lines, and are substantially wider than lines in said interconnecting metalization structure.

33. The structure of claim 31 wherein said metal interconnecting lines are power buses, and are substantially wider than lines in said interconnecting metalization structure.

34. The structure of claim 31 wherein said metal interconnecting lines are ground buses, and are substantially wider than lines in said interconnecting metalization structure.

35. The structure of claim 31 wherein said metal interconnecting lines are a combination of signal lines and power buses, and are substantially wider than lines in said interconnecting metalization structure.

36. The structure of claim 31 wherein said metal interconnecting lines are a combination of power and ground buses, and are substantially wider than lines in said interconnecting metalization structure.

37. The structure of claim 31 wherein said metal interconnecting lines are a combination of signal and ground buses, and are substantially wider than lines in said interconnecting metalization structure.

38. The structure of claim 29 wherein the size of said contact points is within the range of approximately 0.3 um. to 5.0 um whereby further whereby said contact points can comprise any appropriate contact material, such as but not limited to tungsten, copper (electroplated or electroless), aluminum, polysilicon, or the like.

39. The structure of claim 29 wherein said passivation layer comprises a layer within the range of approximately 0.15 to 2.0 um Plasma Enhanced CVD (PECVD) oxide over which a layer within the range of approximately 0.5 to 2.0 um PECVD nitride is deposited.

40. The method of claim 29 wherein said insulating, separating layer is a polymer dielectric layer or any other appropriate insulating material.

41. The method of claim 29 wherein said insulating, separating layer comprises polyimide.

42. The method of claim 29 wherein said insulating, separating layer comprises the polymer benzocyclobutene (BCB).

43. The structure of claim 29 wherein said insulating layer is of a thickness after curing within the range of approximately 1.0 to 30 um.

44. The structure of claim 29 wherein said openings have an aspect ratio within the range of approximately 1 to 10.

45. The method of claim 29 wherein said metal conductors within said openings through said insulating layer and through said passivation layer connecting said electrical contact pads of said top metalization structure with contact points of said interconnecting metalization structure are constructed and routed such that each said electrical contact point of said interconnecting metalization structure is connected directly and sequentially with one electrical contact point of said top metalization structure thereby creating a fan-out effect for said electrical contact point of said interconnecting metalization structure whereby the distance between said electrical contact points of said top metalization structure is larger than the distance between said electrical contact points of said interconnecting metalization structure by a measurable amount.

46. The method of claim 29 wherein said the number of said electrical contact pads of said upper metalization structure can be larger than the number of said contact points of said interconnecting metalization structure by a considerable and measurable amount.

47. The method of claim 29 wherein said metal conductors within said openings through said insulating layer and through said passivation layer connecting said electrical contact points of said top metalization structure with said contact points of said interconnecting metalization structure are constructed and routed such that each said electrical contact point of said interconnecting metalization structure is connected directly but not necessarily sequentially with one electrical contact point of said top metalization structure thereby creating a pad relocation effect for said electrical contact points of said interconnecting metalization structure whereby the distance between said electrical contact points of said top metalization structure is larger than the distance between said electrical contact point of said interconnecting metalization structure by a measurable amount whereby furthermore the sequence or adjacency of said electrical contact points of said interconnecting metalization structure is not necessarily the same as the sequence or adjacency between said electrical contact points of said top metalization structure.

48. The method of claim 29 wherein said metal conductors within said openings through said insulating layer and through said passivation layer connecting said electrical contact points on a top surface of said top metalization structure with contact points of said interconnecting metalization structure are constructed and routed such that functionally identical electrical contact points of said interconnecting metalization structure are inter-connected and are connected with one electrical contact point or fewer elec-

trical contact points of said top metalization structure thereby creating a reduction effect for said electrical contact points of said interconnecting metalization structure whereby the number of contact points for a particular electrical function within said electrical contact points of said top metalization structure is smaller than the number of said electrical contact points of said interconnecting metalization structure by a measurable amount whereby furthermore the sequence or adjacency of said electrical contact points of said interconnecting metalization structure is not necessarily the same as the sequence or adjacency between said electrical contact points of said top metalization structure.

49. A method for forming a top metalization system for high performance integrated circuits, comprising:

forming an integrated circuit comprising a plurality of devices formed in and on a semiconductor substrate, with an overlaying interconnecting metalization structure connected to said devices and comprising a plurality of first metal lines;

depositing an insulating, separating layer over said semiconductor substrate;

forming openings through said insulating, separating layer to expose upper metal portions of said interconnecting metalization structure;

depositing metal contacts in said openings; and

forming said top metalization system connected to said interconnecting metalization structure, wherein said top metalization system comprises a plurality of top metal lines, in one or more layers, having a width substantially greater than said first metal lines.

50. The method of claim 49 wherein said top metalization system comprises signal lines that are substantially wider than lines in said overlaying interconnecting metalization structure.

51. The method of claim 49 wherein said top metalization system comprises power buses that are substantially wider than lines in said interconnecting metalization structure.

52. The method of claim 49 wherein said top metalization system comprises ground buses that are substantially wider than lines in said interconnecting metalization structure.

53. The method of claim 49 wherein said top metalization system comprises planes that contain both signal lines and power buses that are substantially wider than lines in said interconnecting metalization structure.

54. The method of claim 49 wherein said top metalization system comprises planes that contain both signal lines and ground buses that are substantially wider than lines in said overlaying interconnecting metalization structure.

55. The method of claim 49 wherein said top metalization system comprises planes that contain both power buses and ground buses that are substantially wider than lines in said overlaying interconnecting metalization structure.

56. The method of claim 49 wherein said overlaying interconnecting metalization structure comprises electrical contact points whereby said contact points can comprise any appropriate contact material, such as but not limited to tungsten, copper (electroplated or electroless), aluminum, polysilicon, or the like.

57. The method of claim 56 wherein the size of said contact points is within the range of approximately 0.3 um. to 5.0 um.

58. The method of claim 49 further comprising depositing a passivation layer over said interconnecting metalization structure.

59. The method of claim 58 wherein said passivation layer comprises Plasma Enhanced CVD (PECVD) oxide.

60. The method of claim 58 wherein said passivation layer comprises Plasma Enhanced CVD (PECVD) nitride.

61. The method of claim 49 wherein said insulating, separating layer is a polymer dielectric layer or any other appropriate insulating material.

62. The method of claim 49 wherein said insulating, separating layer is s elected from the group comprising polyimide and benzocyclobutene (BCB).

63. A method for forming a top metalization system for high performance integrated circuits, comprising: forming an integrated circuit comprising a plurality of devices formed in and on a semiconductor substrate, with an overlaying interconnecting metalization structure connected to said devices and comprising a plurality of fine-wire metal lines;

depositing a passivation layer over said interconnecting fine-wire metalization structure;

depositing an insulating, separating layer over said passivation layer that is substantially thicker than said passivation layer;

forming openings through said insulating, separating layer to expose upper metal portions of said overlaying interconnecting metalization structure;

depositing metal contacts in said openings thereby raising a plurality of contact points in said overlaying interconnecting metalization structure to the top surface of said insulating, separating layer thereby creating elevated interconnecting metalization contact points;

forming said top metalization system connected to said overlaying interconnecting metalization structure, wherein said top metalization system comprises a plurality of top wide-metal lines, in one or more layers, having a width substantially greater than said fine-wire metal lines, wherein said top metalization system directly interconnects said elevated interconnecting metalization contact points thereby functionally extending or connecting said fine-wire metal interconnects with said wide-wire metal interconnects thereby furthermore establishing electrical interconnects between multiple points within said fine-wire interconnects.

64. The method of claim 63 wherein said top metalization system comprises signal lines that are substantially wider than lines in said interconnecting metalization structure.

65. The method of claim 63 wherein said top metalization system comprises power planes that are substantially wider than lines in said interconnecting metalization structure.

66. The method of claim 63 wherein said top metalization system comprises ground planes that are substantially wider than lines in said interconnecting metalization structure.

67. The method of claim 63 wherein said passivation layer comprises Plasma Enhanced CVD (PECVD) oxide.

68. The method of claim 63 wherein said passivation layer comprises Plasma Enhanced CVD (PECVD) nitride.

69. The method of claim 63 wherein said insulating, separating layer is a polymer dielectric layer or any other appropriate insulating material.

70. The method of claim 63 wherein said insulating, separating layer comprises polyimide.

71. The method of claim 63 wherein said insulating, separating layer comprises the polymer benzocyclobutene (BCB).

72. The method of claim 63 wherein said insulating, separating layer is of a thickness after curing within the range of approximately 1.0 to 30 um.

73. The method of claim 63 wherein said insulating, separating layer is spin-on coated and cured.

74. The method of claim 63 wherein said openings have an aspect ratio within the range of approximately 1 to 10.

75. The method of claim 63 wherein said metal contacts is selected from the group comprising sputtered aluminum, CVD tungsten, CVD copper, electroplated copper, electroless nickel and damascene metal filling.

76. The method of claim 63 wherein said openings through said insulating, separating layer have sloped sides and wherein each of said openings is wider at its top.

77. The method of claim 63 thereby furthermore functionally and physically extending said top metalization system connected to said overlaying interconnecting metalization structure, wherein said top metalization system comprises a plurality of ground planes, in one or more layers, wherein furthermore said overlaying interconnecting metalization structure directly interconnects a multiplicity of ground wires said ground wires to be connected with fine-wire ground wires thereby functionally extending or connecting said fine-wire ground wire metal interconnects with said wide-wire metal ground wire interconnects contained within said top metalization system thereby extending the fine-wire ground wires as contained within the overlaying interconnecting metalization structure with said top metalization system.

78. The method of claim 63 thereby furthermore functionally and physically extending said top metalization system connected to said overlaying interconnecting metalization structure, wherein said top metalization system comprises a plurality of signal planes, in one or more layers, wherein furthermore said overlaying interconnecting metalization structure directly interconnects a multiplicity of signal wires said signal wires to be connected with fine-wire signal wires thereby functionally extending or connecting said fine-wire signal wire metal interconnects with said wide-wire metal signal wire interconnects contained within said top metalization system thereby extending the fine-wire signal wires as contained within the overlaying interconnecting metalization structure with said top metalization system.

79. The method of claim 63 thereby furthermore functionally and physically extending said top metalization system connected to said overlaying interconnecting metalization structure, wherein said top metalization system comprises a plurality of power planes, in one or more layers, wherein furthermore said overlaying interconnecting metalization structure directly interconnects a multiplicity of power wires said power wires to be connected with fine-wire power wires thereby functionally extending or connecting said fine-wire power wire metal interconnects with said wide-wire metal power wire interconnects contained within said top metalization system thereby extending the fine-wire power wires as contained within the overlaying interconnecting metalization structure with said top metalization system.

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RELATED PROCEEDINGS APPENDIX

None